BROCHURE

ASIC ARCHITECT

High Speed Interface Controllers

Company

ASIC Architect, Inc. is a high speed interface controller company. Based in Santa Clara, California, the heart of Silicon Valley, the company strives to provide the best products, support and services to its clients world-wide. In high technology area, focus is the key to success. And it is the focus that translates into high quality of our products and services.

Currently, the company has products and services in PCI Express and DDR I/II Controllers area. In addition to the main products, the company also provides solution cores around its main core products that accelerates your chip-level integration, and results in shorter time to market window.

ASIC Architect understands the criticality of first-pass silicon success and works closely with its customers all the way from cire integration through silicon. Our products and services are targeted and tailored towards networking, storage, wireless and consumer product markets.

Product Portfolio

PCI EXPRESS

- End point Cores
- Root Port Cores
- Dual Mode - Root/ Endpoint Cores
- Switch Port Cores

DDR

- DDR I Controller Core
- DDR II Controller Core

SOLUTION PRODUCTS

- PCI Express 4-port Configurable Switch
- PCI Express Memory Completer Core
- DMA Engines
- ECC Core
- DDR I/II Controller Multiple Client Servicing Cores
- Physical Coding Subystem Logic Core

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ASIC ARCHITECT

DATA SHEET

PCI Express IP Cores

Endpoint, Root Port, Switch Port and Dual Mode Cores

PCI EXPRESS®

Low Silicon Footprint, Low Latency and Maximum Throughput Cores

PCI Express IP Core Overview

ASIC Architect's high performance cores come in multiple datapath flavors with the choice of 8-bit or 16-bit PIPE PHY Interface. The cores have been architected to achieve very low latency, high throughput, and quick timing closure with a very small silicon footprint. The user interface provides practical and integration-friendly mechanisms for the integration of the cores to the user logic.
Our PCI Express products support the most advanced features - Power Management, QoS, Hot-Plug & Hot-Swap, Data Integrity, Trusted Integration and Error Handling.

Please refer to the product matrix below to choose the core for your ASIC/FPGA.

PCI Express Specification Supported

- PCI Express Specification 1.1 (Gen 1)
- PCI Express Specification 2.0, Rev 0.7 (Gen 2)

Architecture

- Architected by industry veterans with SoC expertise
- Highly Scalable & Pipelined Architecture
- Easily configurable Plug-and-Play User Logic Interface
- Optimized architecture with multiple datapath widths
- Design for Testability (DFT) and Design for Debugability (DFD) features
- Technology independent design for ASIC/FPGA
- Excellent integration with PIPE or Non-PIPE PHY logic

Highlights

ASIC Architect's PCI Express IP Cores are silicon-proven, highly configurable, scalable and ready to meet your custom design requirements.

- High Performance with Low Latency, Maximum Throughput, Multiple Pipelined Memory WR/RD capability
- Low Silicon Footprint - Suitable for Multiple Instances of the Core in Single ASIC/FPGA
- Highly Parameterized Core supporting both cut-through and store-and-forward schemes
- Supports operation with 8-bit and 16-bit PIPE interface
- Implements all optional configuration space and capability structures
- Configurable Retry buffering scheme for low footprint and latency
- Supports all power management states L0,L0s,L1,L2 & L3
- Supports PCI Express Advanced Error Reporting

ASIC Architect's PCI Express solutions are backed by a strong team of engineers whose core focus is in High Speed Controller domain.

PCI Express Solution Cores

- Four port Configurable PCI Express Switch
- DDR I/II Memory Controller Core
- DMA Controller Core
- Slave Mode Memory Controller Core
- PCS Logic Core

PCI Express Datapath Flavors

PCI Express Cores	x8	x4	x2	x1	x16
Endpoint	64/128 bit	32/64/128 bit	32/64/128 bit	32/64/128 bit	128 bit
Root Port	64/128 bit	32/64/128 bit	32/64/128 bit	32/64/128 bit	128 bit
Dual Mode (EP/RC)	64/128 bit	32/64/128 bit	32/64/128 bit	32/64/128 bit	128 bit
Switch Port (Upstream/Downstream)	64/128 bit	32/64/128 bit	32/64/128 bit	32/64/128 bit	128 bit

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High Performance, Feature-Rich Soft IP Cores

Low Silicon Footprint, Low Latency and Maximum Throughput Cores

Reliability

- Silicon Proven Design
- Design for Testability and Design for Debugability
- Added in the PCI-SIG PCI Express Integrators List
- Thoroughly verified against industry leading PCI Express verification suites
- Extensive list of Interoperable PCI Express vendors

Plug and Play type Application Interface

- Easy-to-Integrate Interface with User Logic
- Streamlined User Interface with reasonable number of interface signals
- Controllability for critical device parameters

Design for Testability/ Design for Debugability

- Allocate infinite credits
- Bypass credit check
- Optional parity protection for Datapath and RAM

Parameterized Core

- Highly Parameterized RTL for easy configurability depending on your custom requirements
- Supports both Cut-Through and Store-and-Forward schemes for forwarding transmitted packets
- Core operates at all allowed speeds down to x1 mode
- User configurable Virtual Channels and Traffic Class mapping
- Selectable ECRC and Advanced Error Reporting Support
- Configurable Type-0 (Endpoint) or Type-1 (Root Port, Switch Port) Config Headers

High Performance

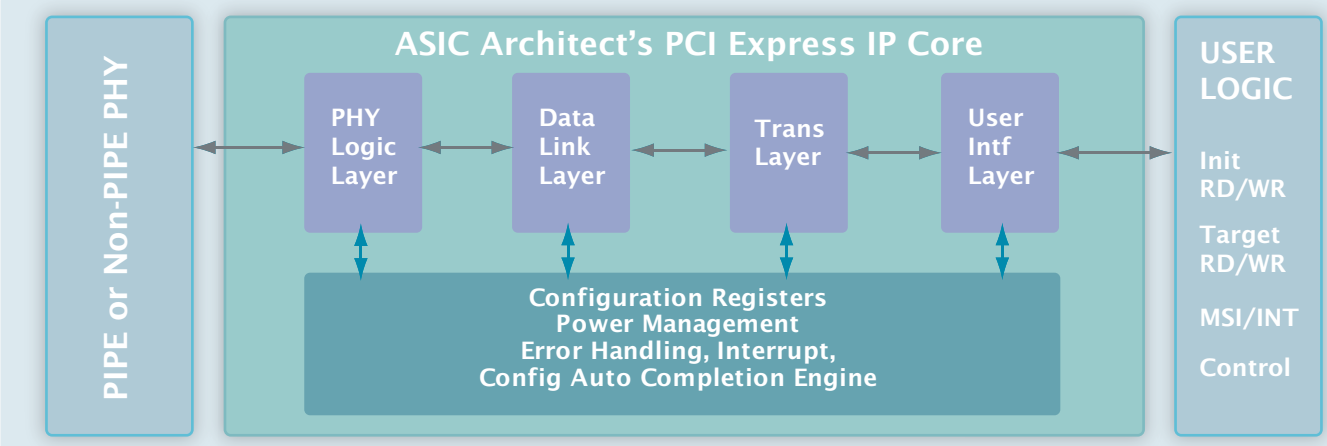
- Supports upto 8 Virtual Channels and 8 Traffic Classes
- Full Isochronous Traffic Support
- Multiple Pipelined Memory Read Capability
- Highly Configurable Retry buffer design for low latency and area depending on user application
- Pipelined/Streaming Operation for Memory Write Requests
- Very Low Transmit and Receive Latency
- Low Silicon Footprint
- Non-Blocking Architecture
- Maximum PCI Express Link Utilization
- Complete Power Management Support
- Multifunction Endpoints

Power Management Features

- Supports all required and optional PCI Express Power Management features
- Supports Beacon and Wake-Up mechanism
- Supports all PM states L0, L0s, L1, L2 & L3
- ClkREQ mechanism for low power mode in mobile form factors

ASIC / FPGA Deliverables

- Synthesizable Verilog RTL
- Testbench and Models for Simulation
- Sample Synthesis Scripts (for ASIC)
- User Constraint File (for FPGA)
- Sample Static Timing Analysis
- User Manual for Integration and Application Notes
- Support from Core Integration through Silicon Bring-Up



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DATA SHEET

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DDR I/II Controller Core

Low Silicon Footprint, Low Latency and Maximum Throughput Cores

Product Overview

ASIC Architect's DDR I/II Controller Core is an integral part of the product portfolio aimed at providing a complete end-to-end solution in the High Speed Interface Controller domain. The DDR I/II Controller Core has been architected, designed and verified by ASIC/SoC industry veterans. The add-on solution cores that come with the DDR Controller accelerate the chip-level integration by connecting multiple clients to the DDR Controller.

Product Features

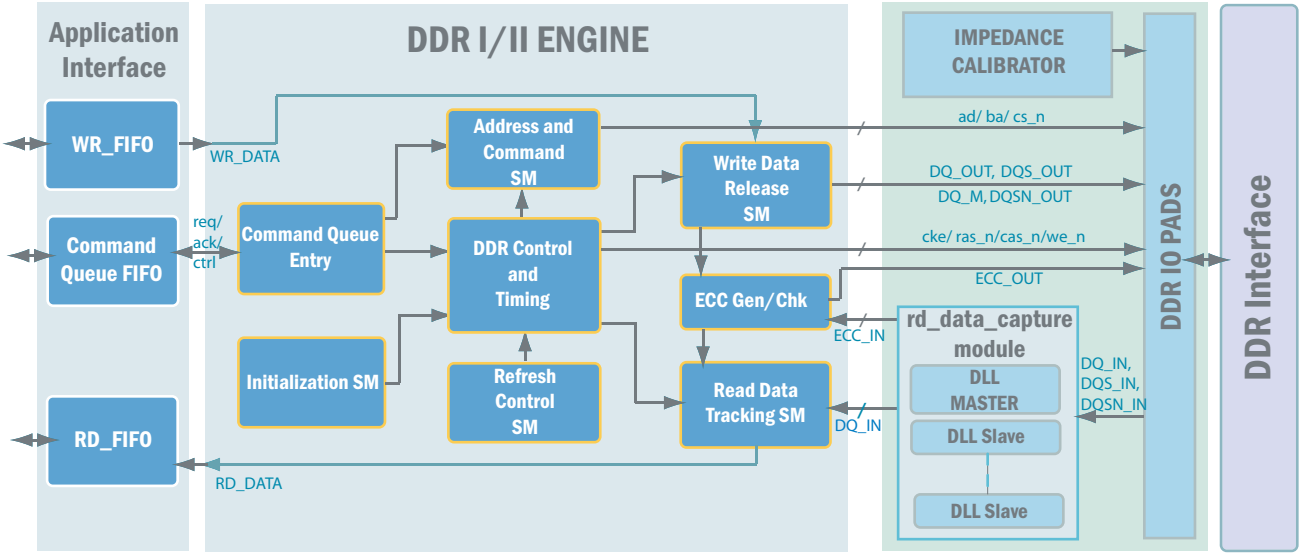
- Powerful Application Interface
- Supports both DDR I and DDR II JEDEC Standards
- Addressing capability upto 4GB DDR2 devices
- Programmable Features:
  - Memory timing parameters - Tras, Trdl, Twr, Tccd, Trfc, Tmrd, Trp, Tcrd
- Intelligent Bank Management
- Supports buffered and unbuffered DIMMs
- Supports On-die termination (ODT), and Off-Chip Driver impedance adjustment
- Configurable Features:
  - Address Mapping between application bus and row/column/bank addresses
  - Choice of 16/32/64-bit DDR bus-width
  - Size of Command Queue
- Supports addition CAS latency feature to maximize command bus utilization
- Supports Back-to-Back WR & RD with minimum time intervals

Product Features

- High data rate upto 100% memory throughput
- Byte-wide optional ECC Support
- Auto initialization of DDR Memories
- Byte-Wide Data Mask Support
- Self-refresh and power down control
- Fully ATPG Testable - Multiple Clock Domains
- Supports upto 800MHz in DDR II Mode
- Supports industry standard memory vendors
- Low Gatecount
- Low Latency
- Verified with leading memory and IO vendors
- Supports Multiple Application Clients

ASIC Deliverables

- Synthesizable Verilog RTL
- Testbench and Models for Simulation
- Complete User Integration Manual
- Sample Synthesis and Static Timing Analysis Scripts
- Support from Core Integration through Silicon Bring-Up



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