Amber Path FX

SPICE Accurate Statistical Timing for 40nm and Below

Amber Path FX is a trusted analysis solution for designers trying to close on power, performance, yield and area in 40 nanometer processes and below. Amber Path FX is

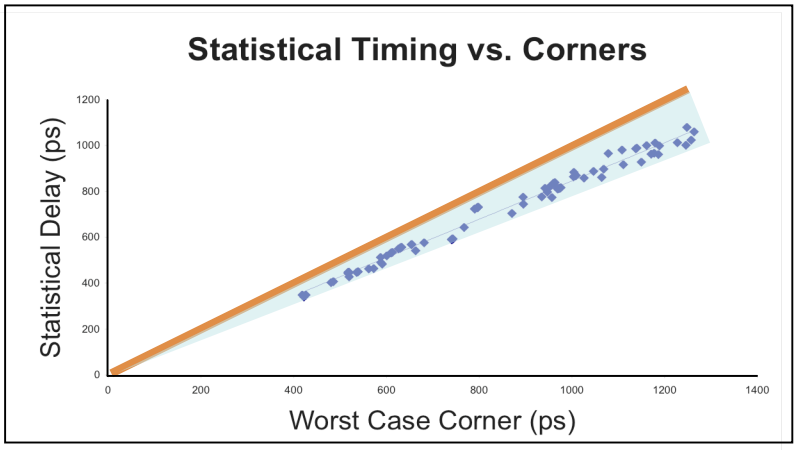
- Accurate: Developed with TSMC for 40nm vs. SPICE for delay and variance.
- Fast: Evaluate 10's of 1000's of paths per hour; 100,000x faster than Monte Carlo SPICE
- Practical: Works directly with PrimeTime™ and adapts easily to existing design flows.

Traditional timing tools waste ≈20% of the timing margin in a 40nm design. SPICE and Fast SPICE Monte Carlo solutions provide the accuracy needed for sign-off, but they lack the performance to address even a small fraction of the critical paths in a design. Much of the value of today's advanced processes is effectively 'left on the table.'

Amber Path FX enables design teams to recapture timing margin and apply it to reducing power, increasing clock frequency, centering a design for yield, shrinking area, or simply making the determination a chip is ready for tape-out.

Traditional Sign-Off Wastes ≈20% of the Timing Margin at 40nm

The pessimism of timing corners at smaller geometries is well documented. Process corners exaggerate extremely low probability events. A very low probability increase in variance appears as a very large spread in design corners. The worst case to best case spread has increased to where a 40nm process can seem slower than a 55nm process.



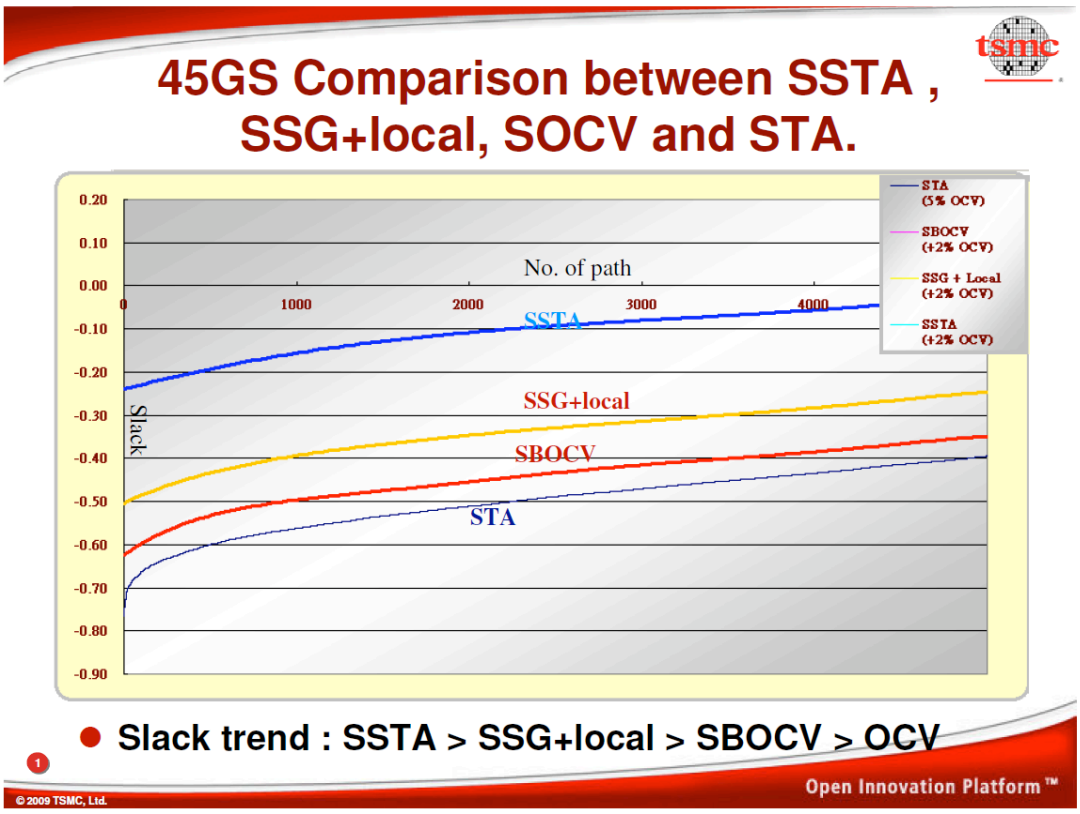
A much better metric for manufacturing variance is the true statistical spread, or 3 sigma value relative to the mean. A higher sigma indicates a higher probability that a path will meet a given timing value. At 3σ there is a 99.87% probability the path will meet that timing. As the figure illustrates, the magnitude of the spread between the true 3 sigma variance of a 40nm process with the corner based timing. As this sample of path delays shows, corner based analysis is significantly more pessimistic than the true manufacturing distribution.

The triangular area between the red line or 3 sigma delay, and the scatter plot of corner delays is the lost margin. The additional margin present in the circuit could be used to improve clock frequency, power, yield, or simply to waiver paths prior to tape-out.

The Margin Gap cannot be fixed with OCV or SBOCV

One proposal is to use On Chip Variation (OCV) or Stage Based OCV (SBOCV) as a means of recapturing some of the margin lost to corners. Aside from the challenges of calculating OCV or SBOCV values (which themselves take many days of SPICE runs), the reality is that these methods do little to close the gap.

The following figure compares statistical approaches with STA OCV, and STA SBOCV. Again, the OCV based approaches only make a small incremental improvement in the predicted slack. In comparison, the statistical estimate provides a material difference in expected slack, often in the range of 100s of picoseconds on real designs.



Traditional SPICE and Fast SPICE are too slow

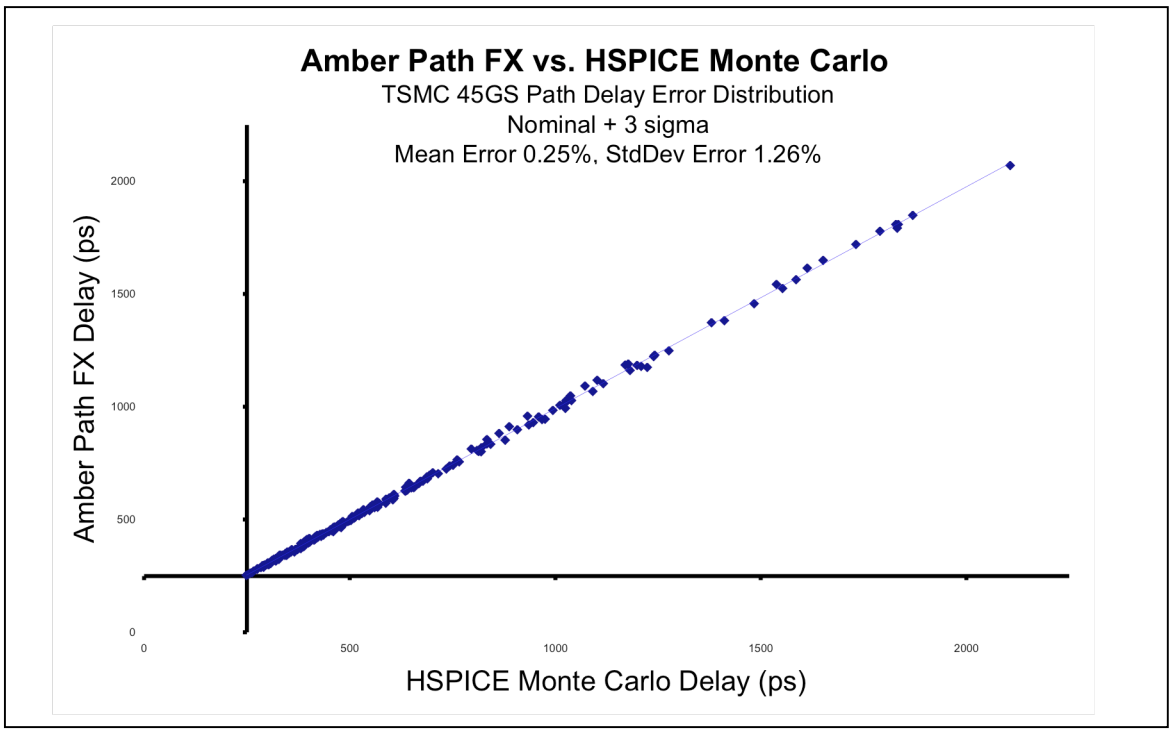
The challenge is to find a SPICE accurate tool for delay and statistical variance that is fast enough to evaluate enough of the design to recapture lost margin. The traditional approach of using SPICE or Fast SPICE to evaluate critical paths is too time consuming and expensive. Monte Carlo SPICE on a single complex path can take upwards of 500 hours. A Fast SPICE approach might reduce this to a few hours per path. Considering that a design may have 1000s of failing paths, these approaches are simply impractical.

Amber Path FX: Accurate, Fast, Practical

Amber Path FX, developed in conjunction with TSMC, is a statistical timing solution for 40nm and below. It is SPICE accurate, fast and practical. It uniquely combines the performance, trusted answers, and methodology required to address the limitations of existing SPICE and static timing solutions.

Accurate: Developed with TSMC for 40nm vs. SPICE

Amber Path FX was developed in conjunction with TSMC, for the TSMC 40nm processes and libraries. The FX models are transistor based and are characterized directly from the TSMC cell level SPICE netlists and BSIM models.



The above figure compares the accuracy of Amber Path FX with SPICE using TSMC 45nm libraries. Several hundred complex test paths (as measured by fanout, depth and cell complexity) are shown here. The path includes data, launch clock and capture clock. This figure compares nominal plus 3 sigma. Over 98% of the paths are within 2% of nominal and nominal plus 3 sigma.

Fast: 100,000x Faster than Monte Carlo SPICE

Amber Path FX can evaluate 1000s of paths per hour with SPICE accuracy. Averaging seconds per core for full statistical timing of an entire path (clock and data), Amber Path FX is fully threaded to take maximum advantage of multi-processor systems. Amber Path FX uses an advanced Variance Solver for statistical calculations that eliminates the computational bottleneck of traditional Monte Carlo methods.

With 40nm and 28nm BSIM models now including as many as 20 Global, and 5 local variables to represent variance, Monte Carlo approaches cannot keep up. An increase in the number of variables increases Monte Carlo run times *geometrically*. With the Amber Path FX Variance Solver, the impact is *linear*.

Moreover, generation of the FX transistor model takes just hours, compared with weeks for the less accurate CCS and ECSM libraries used by most STA tools. With the number of statistical parameters in the BSIM SPICE models steadily increasing, this differential will only get greater.

Practical: Works directly with PrimeTime™ in Existing Design Flows

Amber Path FX works directly with PrimeTime™, PrimeTime SI™, and with PrimeTime/Celtic design flows. A small script is added to an existing PrimeTime run to capture all of the data necessary to drive Amber Path FX. This script exports all of the information concerning paths of interest (for example paths with slack less than X), and in the case of PrimeTime SI, and PT Celtic flows, the incremental signal integrity delays.

The timing reports have been designed to be as familiar as possible to the typical engineer. They capture all of the additional information generated by Amber Path FX and present them in a standard timing report format.

Amber Path FX can export SDF for all evaluated paths. This SDF can be fed back into PrimeTime, or into a physical design tool for optimization. The optimization tools can then focus on far fewer failing paths (if any) or target paths with sufficient margin for power reduction.

Amber Path FX supports S SPEF for statistical parasitic calculations as defined by Si2. This allows the delay calculation to incorporate statistical metal variation as well gate variation. The user must have an extracted S SPEF file for inclusion into the analysis.

TSMC Support

FX models for TSMC's core 40nm libraries are available directly from TSMC upon special request. Amber Path FX was developed in conjunction with TSMC for the TSMC 40nm processes and libraries. CLK works closely with TSMC on every step of the design flow, from library characterization, use models, reports, to special applications.

The FX models are transistor based and are characterized directly from the TSMC cell level SPICE netlists and BSIM models. Amber Path FX reads in the extracted SPICE netlist for each cell, characterizes each transistor in the netlist, and then re-instantiates the full cell including parasitics.

Because FX models can be generated in a few hours, TSMC's FX libraries are always up to the minute with the latest SPICE BSIM model information. For final sign-off or late stage process revisions, the FX model is always in sync with the latest data from the TSMC fabs.

The FX Model

Amber Path FX's accuracy comes from the FX model. FX is a transistor level model which can be used to calculate timing and variance. The FX model is used to create transistor level representations of each of the cells in a library directly from the extracted SPICE netlists and TSMC BSIM SPICE model.

The FX transistor level model has substantial advantages over traditional arc models such as NLDM, ECSM and CCS. Arc based models simply miss many of the critical delay and variance effects. FX, by using a transistor model in a netlist to model each cell, has all the same advantages of a true SPICE representation.

- Full waveform propagation through all stages of path for correct slew, delay & variance
- Single model for delay, variance, noise and power
- Ability to handle multiple-input switching, noise on delay, glitch
- Ability to handle local voltage & temperature
- Proper modeling of miller capacitances, resistive networks, nonlinear effects
- Proper modeling of long statistical tails and the full active device range
- Proper propagation of complex waveforms

Amber Path FX allows path delay to be calculated using all, some or none of the TSMC BSIM variance variables. The TSMC SPICE model has Global and Local variance variables. Global variables refer to die to die variance. Local variables refer to on die variance. In addition, with additional characterization specific process points can be timed. Amber allows:

- Nominal only processing for SPICE accurate nominal delay
- Statistical timing with Global and Local variables
- Statistical timing with Local only variables around a fixed process corner

For additional information, please contact: sales@clkda.com, 978.486.1056 ext. 201

CLK Design Automation, Inc.
295 Foster Street
Littleton, MA 01451
www.clkda.com

Amber is trademark of CLK Design Automation. All other trademarks or registered trademarks are property of their respective owners.