

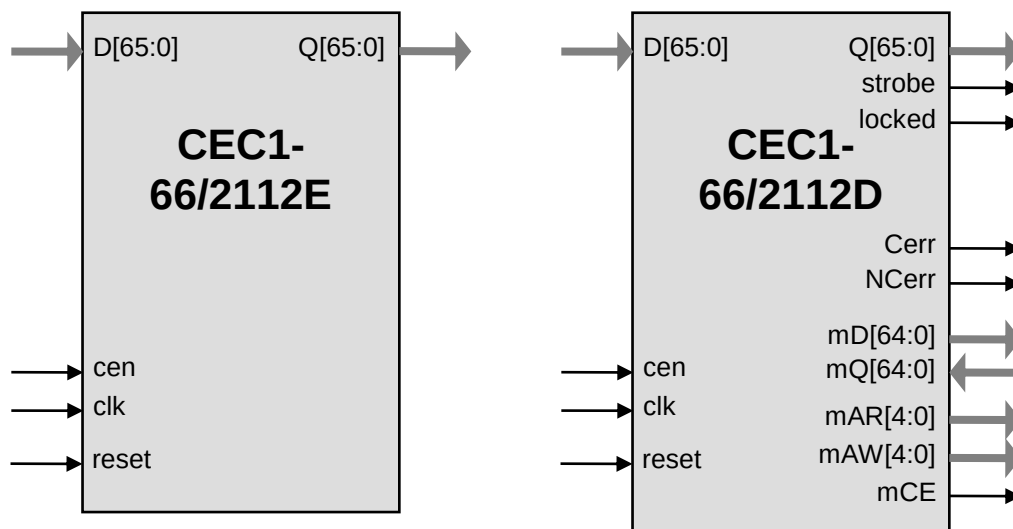
General Description

The CEC1-66/2112 core implements the codec for the Forward Error Correction (FEC) cyclic code (2112,2080) used in the IEEE 802.3ap (10G Backplane Ethernet) standard and IEEE 802.3ba (40 Gbps/100 Gbps operation). The encoder and decoder functions are completely independent and packaged as two sub-cores, CEC1-66/2112E and CEC1-66/2112D respectively. Decoder corrects a single burst error of upto 11 bits.

Key Features

- Small size
- Implements FEC Sublayer for 10GBASE-R (section 74 of the IEEE 802.3 standard)
- 10G/40G/100G Ethernet MAC-friendly interface
- Practically self-contained: requires only memory for one 2112-bit block in the decoder.
- Flow-through design; low latency

Symbols



Pin Description

Name	Type	Description
clk	Input	Core clock signal
cen	Input	Synchronous enable signal. When LOW the core ignores all its inputs and all its outputs must be ignored.
reset	Input	Asynchronous reset
D[65:0]	Input	Input Data
Q[65:0]	Output	Output Data
mD[64:0]	Output	Output Data to Memory
mQ[64:0]	Input	Input Data from Memory
mAR[4:0]	Output	Memory Read Address
mAW[4:0]	Output	Memory Write Address
mCE	Output	Memory Clock Enable (duplicates the cen input)
locked	Output	Core has locked to the input data
strobe	Output	Cerr and NCerr outputs are valid
Cerr	Output	Error has been corrected
Ncerr	Output	Uncorrectable errors detected

Function Description

The CEC1-66/2112E core implements the FEC encoder per section 74 of the IEEE 802.3 standard.

The CEC1-66/2112D core implements the FEC decoder per section 74 of the IEEE 802.3 standard.

Export Permits

The core is subject to the US export regulations. See the IP Cores, Inc. licensing basics page, <http://ipcores.com/exportinformation.htm>, for links to US government sites and licensing details.

Deliverables

HDL Source Licenses

- Synthesizable Verilog RTL source code
- Verilog testbench (self-checking)
- Vectors for the testbench
- Expected results
- User Documentation

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