LXP2 Core

High-Performance Lossless Compression Core

General Description

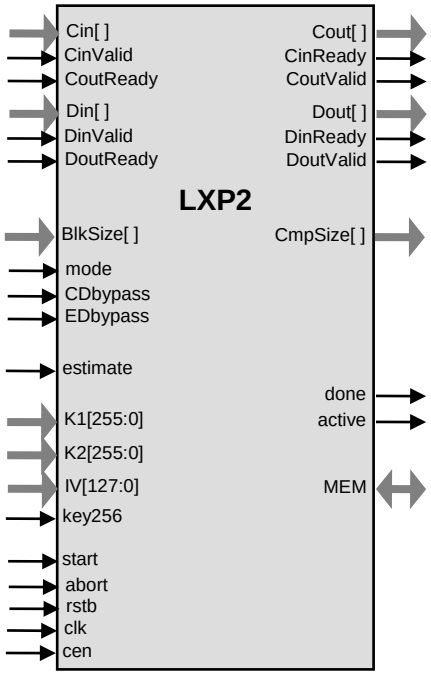
Lossless data compression is a class of data compression algorithms that allows the exact original data to be reconstructed from the compressed data.

LXP2 implements the lossless compression /decompression algorithm and AES-XTS encryption /decryption on units of data (“blocks”). Typical applications include enterprise data storage.

The design is fully synchronous and available in multiple configurations varying in bus widths and throughput.

LXP2 delivers 1-3 Gbps of throughput in both FPGA and ASIC implementations. The compression ratio greatly depends on the data and somewhat depends on the frames size; on typical file corpuses varies between 1.5 and 2.

Symbol



Key Features

Each frame is compressed and decompressed independently

Compatibility with public-domain LZ software implementations allows for interoperability

Parameterizable maximum block size (up to 16 megabytes)

Support for compression and decompression in a single core; dedicates compression and decompression versions are available

Back-to-back compression with no gaps between the frames

Applications

- High-performance solid-state storage
- Disk and tape storage systems

Pin Description

Name	Type	Description
clk	Input	Core clock signal
abort	Input	HIGH level synchronously resets the core
rstb	Input	LOW level asynchronously resets the core
cen	Input	Clock enable
mode	Input	LOW level for compression/encryption, HIGH for decryption/decompression operation
CDbypass	Input	HIGH level indicates a bypass of the compression/decompression function
EDbypass	Input	HIGH level indicates a bypass of the encryption/decryption function
estimate	Input	HIGH level indicates suppression of the compressed data (Cout).
Cin[31:0]	Input	Input data bus for compression/encryption
CinValid	Input	Data on Cin is valid
CinReady	Output	Core is ready to accept data on Cin
Cout[7:0]	Output	Output data bus for results of compression/encryption
CoutReady	Input	Core can drive data on Cout
CoutValid	Output	Data on Cout is valid
Din[7:0]	Input	Input data bus for decryption/decompression
DinValid	Input	Data on Din is valid
DinReady	Output	Core is ready to accept data on Din
Dout[31:0]	Output	Output data bus for results of decryption/decompression
DoutReady	Input	Core can drive data on Dout
DoutValid	Output	Data on Dout is valid
BlkSize[23:0]	Input	Input data length in bytes minus 1
CmpSize[24:0]	Output	Output data length in bytes minus 1
start	Input	A HIGH pulse starts the new block
done	Output	A HIGH pulse indicates the completion of the block processing
active	Output	A HIGH level indicates the core is busy processing the block
K1[255:0]	Input	128/256-bit AES key. 128-bit key resides in the MSB of this port.
K2[255:0]	Input	128/256-bit tweak key (K_2). 128-bit key resides in the MSB of this port.
key256	Input	When HIGH, the K1 and K2 are 256-bit wide. When low, the keys are 128-bit wide.
IV[127:0]	Input	Initial counter value (location)
MEM		Memory interface

Function Description

The core implements lossless compression / decompression and encryption / decryption of data blocks from 512 bytes up to 16 megabytes in length.

The encryption function supports the XTS-AES encryption (including the CTS feature) per NIST SP800-38E (http://csrc.nist.gov/publications/nistpubs/800-38E/nist-sp-800-38E.pdf).

Performance

On the Calgary corpus with the 4096-byte block the core exhibits the following performance:

File	Compression ratio	File	Compression ratio
bib	1.56 (64.22%)	paper3	1.49 (66.93%)
book1	1.39 (71.97%)	paper4	1.54 (64.83%)
book2	1.58 (63.10%)	paper5	1.59 (62.97%)
geo	1.13 (88.52%)	paper6	1.64 (60.88%)
news	1.51 (66.05%)	pic	4.08 (24.52%)
obj1	1.60 (62.70%)	progc	1.74 (57.59%)
obj2	1.83 (54.53%)	progl	2.13 (46.84%)
paper1	1.61 (62.02%)	progp	2.13 (47.00%)
paper2	1.54 (65.11%)	trans	1.93 (51.73%)

Export Permits

The core is subject to the US export regulations. See the IP Cores, Inc. licensing basics page, http://ipcores.com/exportinformation.htm, for links to US government sites and licensing details.

Deliverables

HDL Source Licenses

- Synthesizable Verilog RTL source code
- Verilog testbench (self-checking)
- Vectors for the testbench
- Expected results
- User Documentation

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