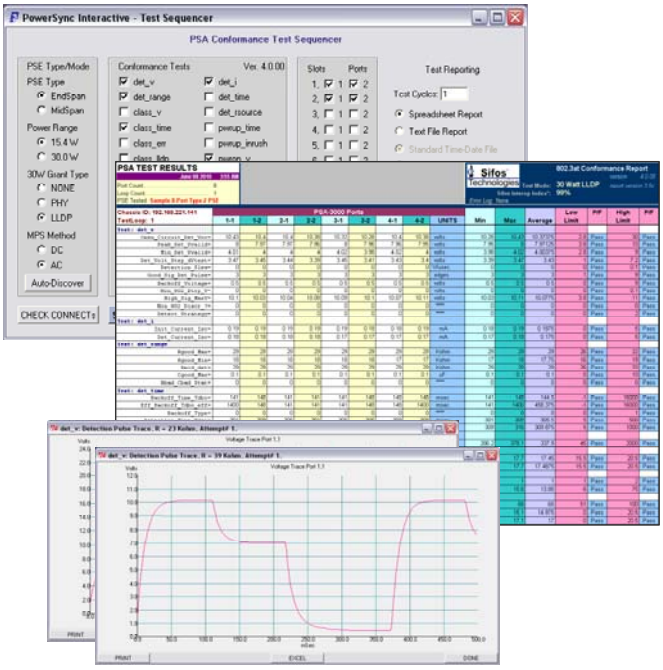
# PSA-CT

## PSE Conformance Test Suite

***for the PSA-3000 PowerSync® Analyzer***




Product Overview

## Key Features

- ❑ **Robust 802.3at (*PoE+*) PSE Compliance Testing**
- ❑ **Fully Automated Port Sequencing and Statistics**
- ❑ **Greater than 95% 802.3at PICS Coverage* from 23 Tests Producing up to 137 Test Parameters per Port**
- ❑ **Fully Emulates All Type-1 (PD Class 0, 1, 2, or 3) and Type-2 (PD Class 4) PD's Including LLDP-Capable PD's**
- ❑ **Adapts to All Prevalent PSE Signaling and Power Behaviors**
- ❑ **Adapts to Prevalent Composite 802.3at and Proprietary Detection Signaling Behaviors**
- ❑ **Configurable Waveform Trace Diagnostic Generation and Retention to 10 Waveforms per Test**
- ❑ **Colorful and Informative Spreadsheet Reporting with Compliance (Pass/Fail) Notations and Parameter Statistics**
- ❑ **Run & Sequence from PSA Interactive GUI or PowerShell PSA Command Line**

## Overview

***The Industry "Norm" for 802.3at PSE Compliance….***

Power-over-Ethernet (PoE) challenges design and test engineers to evaluate multi-channel, "smart" DC power sources that are activated and deactivated through signaling protocols operating over several power delivery and polarity configurations. The application and management of DC power over multiple local area network connections must be completely transparent, safe, non-destructive, and non-disruptive to the traditional data transmission behaviors of those network connections and associated network equipment.

### Higher Power with 802.3at

Under the IEEE 802.3at standard, power delivered to a single Powered Device is effectively doubled to 25.5 watts. PSE's will pack more electrical power and more processing power to manage that electrical power. Issues of safety and specification compliance are accentuated by the higher power delivery capabilities of each Ethernet Port.

***High Coverage of All PSE Functional and Performance Parameters…***

### Smarter PSE's and PD's

In the new 802.3at realm, end-span PSE's such as data switches and routers can use a Link Layer Discovery Protocol (LLDP) to communicate power needs and availability with a new generation of Powered Devices (PD's). This new protocol is a core component of PSE power resource management with granularity to 0.1 watt per Ethernet port.

***Fully Automated One-Button Testing and Reporting….***

### Fully Automated Testing with Very High Test Coverage

The PSE Conformance Test Suite for 802.3at produces over 130 PoE test parameters per PSE port depending upon PSE capabilities. These parameters are measured in 23 distinct tests that may be selected and sequenced across up to 24 PSE ports at a time. The test covers over 95% of the PSE PICS (conformance check list items) in the IEEE 802.3at specification*. The PSE Conformance Test Suite is widely used throughout the internetworking community as the industry "norm" for PSE specification compliance.

***Flexible Emulation of Type-1 and Type-2 Powered Devices….***

### Flexible PD and LLDP Emulation

The 802.3at standard, unlike its 802.3af predecessor, allows for a variety of PSE and PD types including higher power PD's and LLDP-capable PSE's and PD's. As a result, PSE Conformance Testing now requires increased test "cases" to allow for the variety of powering configurations that can arise. The PSE Conformance Test Suite for 802.3at enables each of these test cases so as to assure full test coverage of all PSE types.

### Robust Diagnostics and Reporting

The PSE Conformance Test Suite for 802.3at can automatically sequence to a pop-up spreadsheet report with full color notations of parameter pass/fail status per port and cross-port statistics for each parameter. This report automatically adapts test limits to the test case that is sequenced. Many of the PSE Conformance Tests capture and analyze various voltage and load current "scope" traces in order to evaluate measurement parameters. These traces can be automatically posted to the display, accumulated, and retained until the end of each test for diagnostic purposes. Each trace is individually notated with a description of the trace purpose or measurement parameter.

* *For 802.3at PICS Coverage, see Sifos application note*:
**802.3at PSE PICS Coverage.pdf**

real Power from Sifos

# PSE Conformance Tests & Parameters

## Detection Signaling and Functional Tests

### det_v — Detection Pulse Waveform Parameters

Captures and analyzes PSE detection probe voltages with both valid and slightly non-valid detection signatures.

| | |
|---|---|
| **Voc** | Peak open circuit (disconnected) detection voltage |
| **Vvalid(Max)** | Maximum Detection Step Level with Valid Signature |
| **Vvalid(Min)** | Minimum Detection Step Level with Valid Signature |
| **ΔVtest** | Detection Step Magnitude |
| **Detection Slew** | Detection step slew rate |
| **Good_Sig_Det_Pulse** | Number of Detection Signal transitions |
| **Vbkoff** | Minimum Voltage during detection (ALT B) backoff |
| **Non802_Step_V** | Level of any pre-detection signals |
| **High_Sig_MaxV** | Maximum detection voltage with high detection signature |
| **Non802_Discr?** | Dependence upon Non-802 detection for validity. PSE's that use non-802.3 detection measurements to resolve a valid signature band will report "1". |
| **Detect Strategy** | Reports PSE Detection as one of five known strategies including 802.3at standard, proprietary pre-detection, etc. |

### det_i — Detection Current Limiting

Measures maximum current sourcing capability from a PSE during detection.

| | |
|---|---|
| **Isc(Init)** | Max detection current at minimum detection voltage |
| **Isc(Det)** | Max detection current during detection |

### det_range — Detection Passive Acceptance Range

Assesses the range of acceptable PD signatures and the reliability of valid detection given random connect timing and capacitive loading.

| | |
|---|---|
| **Rgood_Max** | Maximum accepted detection resistance signature |
| **Rgood_Min** | Minimum accepted detection resistance signature |
| **Rmid_det** | MAX (or MIN) detection resistance given random connections |
| **Cgood_Max** | Maximum accepted detection capacitance signature |
| **Rbad_Cbad_Stat** | Power-Up status given a 35Kohm (marginally high) resistive signature with the lowest Capacitive signature rejected by the PSE. |

### det_time — Detection Timing

Measures detection backoff and detection probe timing parameters.

| | |
|---|---|
| **Tdbo** | Detection back-off time (between failed detections) |
| **Tdbo_eff** | Effective back-off time for PSE's that ignore rather than disable detection measurements |
| **Tdet** | 802.3at detection time duration |
| **Tdet_tot** | Total detection time including pre-detection measurements |
| **Backoff_Type** | Reports PSE Detection back-off as one of three known strategies including 802.3at standard and legacy detections |

### det_rsource — PSE Output Resistance during Detection

Measures effective source resistance of PSE port during detection.

| | |
|---|---|
| **Zout** | PSE estimated output impedance during detection |

## Classification Signaling and Functional Tests

### class_v — Classification Voltages

Captures and analyzes PSE classification voltage levels, focusing on only the final classification performed prior to power-up.

| | |
|---|---|
| **Vclass** | Class Pulse Average Voltage with 1 mA class signature |
| **Vclass_min** | Class Pulse Average Voltage with 45 mA class signature |
| **Vmark** | Mark Region Voltage with 4 mA mark signature load |
| **Vmark_min** | Minimum Port Voltage measured over both MARK regions until power-up |

## Classification Signaling and Functional Tests

### class_time — Classification Timing

Captures and analyzes PSE classification signal timing, focusing on only the final classification performed prior to power-up.

| | |
|---|---|
| **Event_Count** | Count of class pulses |
| **Tpdc** | Duration of class pulse given Single-Event Classification |
| **Tcle1** | Duration of first class pulse given 2-Event Classification |
| **Tcle2** | Duration of second class pulse given 2-Event Classification |
| **Tme1** | Duration of first mark interval given 2-Event Classification |
| **Tme2** | Duration from end of second class pulse to power-up given 2-Event Classification |

### class_err — Classification Current Limiting

Evaluates any current limiting applied to classification signals by PSE as well as PSE powering behaviors following overloaded or illegal classification signatures.

| | |
|---|---|
| **Class_lim** | Maximum Class Current before PSE starts to limit Class Current |
| **Vport_CL_lim** | Power-Up response (as Port Voltage) following a current limited classification |
| **Vport_CL_err_1** | Power-Up response (as Port Voltage) following a 55mA (invalid) classification load |
| **Mark_lim** | Minimum Mark Current Supported during 2-event Mark Region - tested at 5.5 mA and 105 mA given 2-Event Classification |
| **Vport_CL_err_2** | Power-Up response (as Port Voltage) following a class signature that changed from Event #1 to Event #2 (asymmetrical signature) |

### class_lldp — LLDP Protocol and Mutual Discovery Testing

Assesses PSE LLDP basic protocol fields, protocol timing, and power request processing for both Type-1 and Type-2 PD's.

| | |
|---|---|
| **PSE_Source_Priority** | Bit Field for PSE Source, Priority, Reserved |
| **PSE_MDI_Pwr_Sup** | Bit Field from legacy TLV for Port Class, MDI Power Support, MDI Power State, Pair Selection, and Reserved |
| **PSE_LLDP_Time_1** | Time from Power-ON state until first LLDP frame received from PSE given Type-1 PD |
| **PSE_LLDP_Type_1** | PSE Type advertised by a PSE given Class 0-3 PD signature |
| **PSE_Echo_Time_1** | Time for PSE to echo back the PD Requested Power level |
| **PSE_Alloc_Pwr_1** | Allocated Power in response to 8.1 W PD Request from a Class 0–3 PD |
| **PSE_Alloc_Time_1** | Time to respond To 8.1 W PD Request with Power Allocated |
| **PD_Power_Adjust_1** | Allocated Power in response to a Change Request from 8.1W to 13W |
| **PSE_Adjust_Time_1** | Time to echo a PD 13 watt PD Change Request |
| **PSE_LLDP_Time_2** | Time from Power-ON state until first LLDP frame received from PSE given Type-2 PD |
| **PSE_LLDP_Type_2** | PSE Type advertised by PSE given Class 4 PD signature |
| **PSE_Echo_Time_2** | Time for PSE to echo back the PD Requested Power level |
| **PSE_Alloc_Pwr_2** | Allocated Power in response to 20.3W PD Request from a Class 4 PD |
| **PSE_Alloc_Time_2** | Time to respond To 20.3 W PD Request with Power Allocated |
| **PD_Power_Adjust_2** | Allocated Power in response to Change Request from 20.3W to 25.5W |
| **PSE_Adjust_Time_2** | Time to echo a PD 25.5 watt PD Change Request |

## Power-Up Processes

### pwrup_time — Power-Up Timing Parameters

Measures power-up rise time and time delay from completion of final detection until power applied.

| | |
|---|---|
| **Trise** | Rise Time from 10% to 90% of Vport |
| **Tpon** | Time from end of detection until power-up - Tpon is measured from the final complete detection probe preceding a power-up |

### pwrup_inrush — PSE Current Limiting Behaviors During Power-Up

Evaluates PSE current limiting and inrush overload tolerance parameters. Assures compliance to 802.3at figure 33-14, $I_{Inrush}$ current and timing limits in the POWER_UP state.

| | |
|---|---|
| **Init_Inrush** | Maximum output current immediately after 1 msec of a severe inrush overload |

## Power-Up Processes

| | |
|---|---|
| **Max_Inrush_c0** | Maximum output current in time interval from 1 to 75 msec given Class 0, 1, 2, or 3 signature |
| **Max_Inrush_c4** | Maximum output current in time interval from 1 to 75 msec given Class 4 signature |
| **Min_Inrush** | Minimum output current while current limiting in time interval from 1 to 50 msec given 30V or higher port voltage |
| **Tinrush** | Duration of current limiting until PSE removes power |
| **Inrush_45m** | Port voltage after 50msec following 45 msec current limiting inrush overload |
| **Max_Init_Inrush** | Maximum output current up to 1 msec given a severe inrush overload |
| **Vinrush** | Average Port Voltage with PSE in current limit and PSA foldback suppression applied |
| **Inrush_Strategy** | Indicator if PSE uses Tinrush timer or Vport to assess the completion of Inrush |

## PSE Powered-On Performance and Processes

### pwron_v — Powered Port Voltage, Ripple, and Noise

Measures PSE port DC and AC voltages in response to minimum and maximum power loads.

| | |
|---|---|
| **Vport_min_N** | Min Port voltage with 0.5 Watt and Pport_Max (PD Class) loading |
| **Vport_max_N** | Max Port voltage with 0.5 Watt and Pport_Max (PD Class) loading |
| **Vpp_ripple_N** | Peak AC Ripple with 0.5 Watt and Pport_Max (PD Class) loading |
| **Vpp_noise_N** | Peak AC Noise with 0.5 Watt and Pport_Max (PD Class) loading |
| **Vtrans_max_N** | Maximum Port Voltage measured during a 5msec load transient from 12mA to Pport_Max / Vport and back. |
| **Vtrans_min_N** | Minimum Port Voltage measured during a 5msec load transient from 12mA to Pport_Max / Vport and back. |

### pwron_pwrcap — PSE Port Power Capacity

Measures the maximum power delivery capability of a PSE port given various PD Classifications.

| | |
|---|---|
| **Pcon_c0** | Maximum output power from PSE Port given Class 0 PD |
| **Icon_0** | Maximum output current from PSE Port given Class 0 PD |
| **Pcon_c1** | Maximum output power from PSE Port given Class 1 PD |
| **Icon_1** | Maximum output current from PSE Port given Class 1 PD |
| **Pcon_c2** | Maximum output power from PSE Port given Class 2 PD |
| **Icon_2** | Maximum output current from PSE Port given Class 2 PD |
| **Pcon_c3** | Maximum output power from PSE Port given Class 3 PD |
| **Icon_3** | Maximum output current from PSE Port given Class 3 PD |
| **Pcon_c4** | Maximum output power from PSE Port given Class 4 PD |
| **Icon_4** | Maximum output current from PSE Port given Class 4 PD |
| **Type-2_Enable** | Verifies > 450 mA continuously available at 80 msec following 2-event power-up for 2-event, Type-2 PSE's *or* verifies >450 mA is not available for LLDP capable Type-2 PSE's prior to negotiation |

### pwron_maxi — PSE Response to Maximum Overloads

The pwron_maxi test evaluates PSE characteristics with respect to the POWER_ON state PI operating current templates in Figure 33-15 of the 802.3at specification.

| | |
|---|---|
| **Ilim_Peak** | Maximum output current tolerated by PSE in time frame of 8 to 75 msec |
| **Ilim_Min_1** | Minimum output current up to 50 msec with 402mA load pulse and foldback suppression applied to assure > 30VDC (Type-1 PD emulation) |
| **Tlim_1** | Time to port shutdown in response to 400 mA overload given Type-1 PD |
| **Vlim_1** | Average port voltage coincident with Tlim_1 measurement |
| **Ilim_Max_1** | Maximum output current from 1 to 75 msec given 700mA load pulse and foldback suppression active given a Type-1 PD |
| **Ilim_Low_V_Tol_1** | Measures time-to-port-foldback given a Type-1 PD with extreme overload |
| **Ktran_lo** | % excursion below 50V given 250usec (fast) overload transient (686 mA) given a Type-2 PSE |
| **Ilim_Min_2** | Minimum output current up to 50 msec with 686mA load pulse and foldback suppression applied to assure > 30VDC given Type-2 PD emulation |
| **Tlim_2** | Time to port shutdown in response to 684 mA overload given Type-2 PD |

## PSE Powered-On Performance and Processes

| | |
|---|---|
| **Vlim_2** | Average port voltage coincident with Tlim_2 measurement |
| **Ilim_Max_2** | Maximum output current from 1 to 75 msec given 860mA load pulse and foldback suppression active given a Type-1 PD |
| **Ilim_Low_V_Tol_2** | Essentially a measure of time-to-port-foldback given a Type-2 PD |

### pwron_overld — PSE Response to Maximum PD Power Transients

The pwron_overld test assesses powered PSE port behaviors with respect to Ipeak, the maximum power overload allowed to a PD as defined in Equation 33-4 of the 802.3at standard.

| | |
|---|---|
| **%Ipeak_N** | Percent of required Ipeak current that is supported over 50msec duration where Ipeak required is defined by Equation 33-4 given a Type-N PD – maximum level verified is 125% |
| **Vport_Ipeak_N** | Min Port Voltage at Ipeak transient pulse given a Type-N PD |
| **Vport_5%DC_N** | Min Port Voltage over 5 seconds with a quantity of 50 msec Ipeak pulse transients separated by 1 second (5% duty cycle) given a Type-N PD |

## MPS Processes for Power Removal on PD Disconnect

### mps_ac_pwrdn — Power Timing and Load Current Impact on AC MPS PSE's

Evaluates power removal timing and DC load tolerance on an AC MPS PSE.

| | |
|---|---|
| **Tmpdo** | Disconnect power-down timing from disconnect event |
| **I_hold_ac** | Maximum DC Load Current tolerated with AC MPS Disconnect Shutdown |

### mps_ac_vf — AC MPS Signaling Characteristics

Measures AC MPS signaling characteristics during the Tmpdo interval.

| | |
|---|---|
| **V_open** | Peak-Peak AC probing voltage following PD Disconnect |
| **V_open_%Vport** | Peak-Peak AC probing voltage expressed as a % Vport_pse |
| **Fp** | AC probing signal frequency following PD Disconnect |
| **AC_MPS_SR** | AC probing signal slew rate |
| **Isac** | Signal current sourced by AC MPS signal generation resource |

### mps_ac_voff — AC MPS Peak Voltage Characteristics

Measures voltage peaks following PD disconnect and power-down events given an AC MPS PSE.

| | |
|---|---|
| **V_open1** | Peak port voltage found after AC MPS power removal event |
| **Vopen_pk** | Peak port voltage found after the PD disconnect event over a period of one second |

### mps_dc_valid — DC MPS Valid Signature Timing Characteristics

Measures intermittent load tolerance thresholds of a DC MPS PSE.

| | |
|---|---|
| **Tmps** | Minimum valid signature ACTIVE time required for DC MPS validity |
| **Duty_Cycle_tol** | PSE power response to valid / invalid load cycling of 16.7% duty cycle |

### mps_dc_pwrdn — Power Timing and Threshold Assessment on DC MPS PSE's

Evaluates power removal timing and DC load requirements on a DC MPS PSE.

| | |
|---|---|
| **I_hold** | Minimum current required to maintain power given DC MPS PSE |
| **Tmpdo** | Disconnect power-down timing from start of invalid signature |
| **Vopen_pk** | Peak port voltage found after the PD disconnect event over a period of one second |

## PSE Power-Down Characteristics

### pwrdn_overld — PSE Response to Non-Current Limiting Overloads

Evaluates PSE handling of non-current limiting overloads in the PSE discretionary region of the PI operating current templates in Figure 33-15 of the 802.3at specification.

| | |
|---|---|
| **Icut_N** | Smallest load current causing power removal in the time frame of Tcut_Max, or less than 75 msec given a Type-N (1 or 2) PSE. |
| **Tcut_N** | Time from start of transient until power removal when measuring Icut_N. |
| **Isoft_N** | Non-Tcut compliant (> Tcut_Max) overload threshold current given a Type-N (1 or 2) PSE. |
| **Tsoft_N** | Time to shutdown if Isoft_N is discovered. |

**pwrdn_time** — **AC MPS Signaling Characteristics**

Evaluates PSE disconnect discharge timing as well as output characteristics during power removal.

| | |
|---|---|
| **Toff** | Power discharge time with hypothetical 320KΩ load. |
| **Cout** | PSE output capacitance during power discharge |
| **Rp** | PSE shunt output resistance during power discharge |

**pwrdn_v** — **AC MPS Peak Voltage Characteristics**

Measures PSE post-power-removal characteristics following an overload shutdown condition.

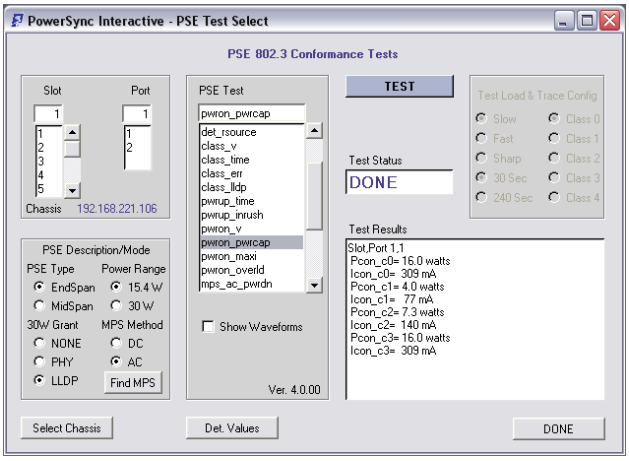
| | |
|---|---|
| **Voff** | IDLE state voltage between detections after overload shutdown |
| **Ted** | Time from overload condition shutdown until a detection probe leading to a successful power-up |
| **Ved** | Peak voltage over the Ted interval |

## Configuring and Running the PSE Conformance Test Suite

The PSE Conformance Test Suite is accessed from either PSA Interactive Software (GUI) or PowerShell PSA, an extended Tcl/Tk command line shell. PSA Interactive provides two menus with access to the PSE Conformance Test Suite: The **PSE Tests** menu and the **Sequencer** menu.

Within each of these menus, users declare:

- PD Emulation: Type-1 (**15.4W**) or Type-2 (**30W**)
- PD 30W Grant Type: **NONE** (Type-1 PSE), **PHY** (Type-2 2-Event PSE), or **LLDP** (Type-2 LLDP)
- PSE Disconnect Detection Method: **AC** MPS or **DC** MPS
- PSE General Type: **End-Span** or **Mid-Span**




**PSA Interactive PSE Tests Menu**

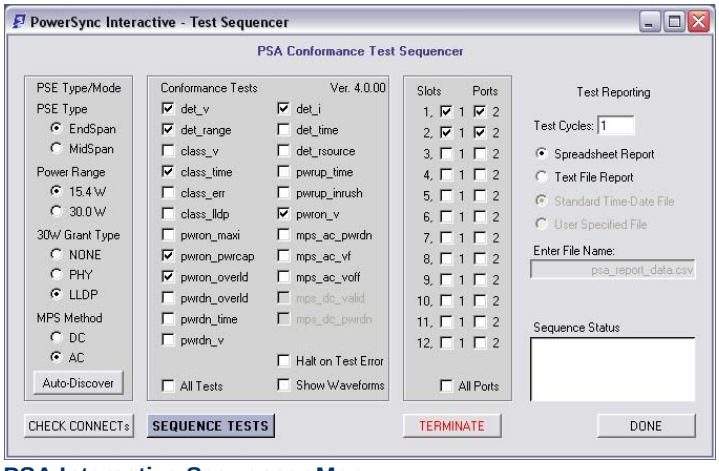
The **PSE Tests** menu is geared to running a single test at a time and capturing results from that test. The menu allows users to select a particular PSA test port (slot and port), then execute a test. Users may optionally select to have any and all measurement waveforms that are used by a given test captured, labeled, and displayed as the test runs.

The **PSE Tests** menu also provides access to certain other specialized testing functions that include user specified loading profiles and LLDP traces.

The **Sequencer** menu allows users to select one or more tests that are to be automatically sequenced along with the PSA test ports that will also be sequenced.

User's may also select one of several reporting options, the most common of which will produce a pop-up (Microsoft Excel) spreadsheet report that performs all test parameter limit checking and analysis.

Multi-Port PSE connections can rapidly be verified prior to testing from this menu and as with the PSE Tests menu, users may opt to have waveform traces produced by each test appear on screen as each test runs. Users may also choose to have the sequence terminate as soon as an error condition develops in any test on any port.




**PSA Interactive Sequencer Menu**

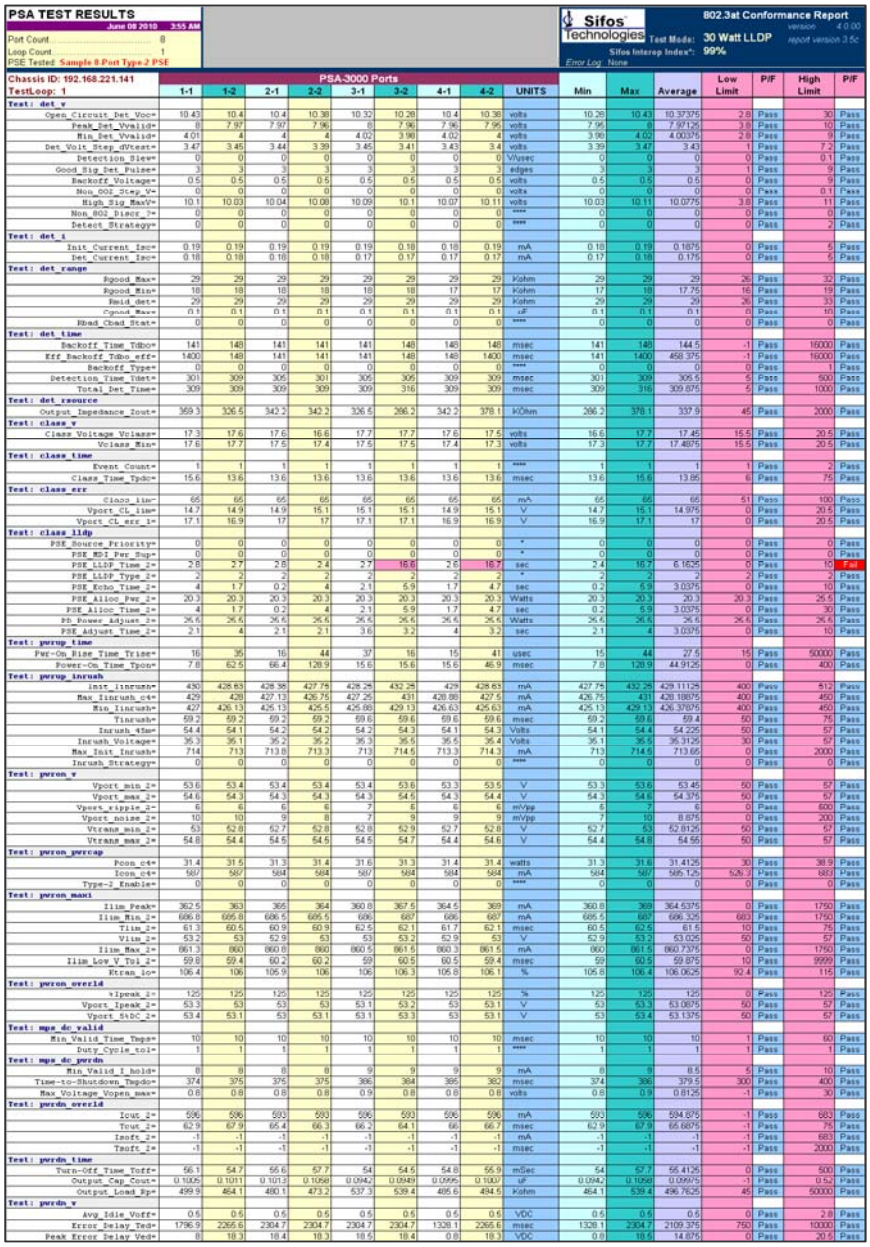
## The PSE Conformance Test Suite Standard Report

The standard spreadsheet test report for the PSE Conformance Test Suite provides efficient feedback by clearly notating any specification compliance violations both by test parameter and by test (PSE) port. The report also accumulates minimum, maximum, and average parameter values across PSE ports so that users can spot individual port deviations and assess performance to design goals.

All test limit processing automatically adapts to the mode of PD Emulation, the type of PSE (e.g. Type-1 or Type-2), and other factors that are specified before the sequence begins.

The report includes one page with detailed explanations of each parameter type and another page that rates the "Interop" Risks of any particular combination of specification violations.

The report will automatically scaled to the number of tested PSE ports.



PSA TEST RESULTS — June 08 2010 3:55 AM
Port Count ..... 8
Loop Count ..... 1
PSE Tested: Sample 8-Port Type-2 PSE

Sifos Technologies — 802.3at Conformance Report (version 4.0.00, report version 3.5c)
Test Mode: 30 Watt LLDP
Sifos Interop Index*: 99%
Error Log: None

Chassis ID: 192.168.221.141
TestLoop: 1

| | PSA-3000 Ports | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | 1-1 | 1-2 | 2-1 | 2-2 | 3-1 | 3-2 | 4-1 | 4-2 | UNITS | Min | Max | Average | Low Limit | P/F | High Limit | P/F |
| **Test: det_v** | | | | | | | | | | | | | | | | |
| Open_Circuit_Det_Voc= | 10.43 | 10.4 | 10.4 | 10.38 | 10.32 | 10.28 | 10.4 | 10.38 | volts | 10.28 | 10.43 | 10.37375 | 2.8 | Pass | 30 | Pass |
| Peak_Det_Vvalid= | 8 | 7.97 | 7.97 | 7.96 | 8 | 7.96 | 7.96 | 7.96 | volts | 7.96 | 8 | 7.97125 | 3.8 | Pass | 10 | Pass |
| Min_Det_Vvalid= | 4.01 | 4 | 4 | 4 | 4.02 | 3.98 | 4.02 | 4 | volts | 3.98 | 4.02 | 4.00375 | 2.8 | Pass | 9 | Pass |
| Det_Volt_Step_dVtest= | 3.47 | 3.45 | 3.44 | 3.39 | 3.45 | 3.41 | 3.43 | 3.4 | volts | 3.39 | 3.47 | 3.43 | 1 | Pass | 7.2 | Pass |
| Detection_Slew= | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | V/usec | 0 | 0 | 0 | 0 | Pass | 0.1 | Pass |
| Good_Sig_Det_Pulse= | 3 | 3 | 3 | 3 | 3 | 3 | 3 | 3 | edges | 3 | 3 | 3 | 1 | Pass | 9 | Pass |
| Backoff_Voltage= | 0.5 | 0.5 | 0.5 | 0.5 | 0.5 | 0.5 | 0.5 | 0.5 | volts | 0.5 | 0.5 | 0.5 | 0 | Pass | 9 | Pass |
| Non_802_Step_V= | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | volts | 0 | 0 | 0 | 0 | Pass | 0.1 | Pass |
| High_Sig_MaxV= | 10.1 | 10.03 | 10.04 | 10.08 | 10.09 | 10.1 | 10.07 | 10.11 | volts | 10.03 | 10.11 | 10.0775 | 3.8 | Pass | 11 | Pass |
| Non_802_Discr_?= | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | **** | 0 | 0 | 0 | 0 | Pass | 0 | Pass |
| Detect_Strategy= | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | **** | 0 | 0 | 0 | 0 | Pass | 2 | Pass |
| **Test: det_i** | | | | | | | | | | | | | | | | |
| Init_Current_Isc= | 0.19 | 0.19 | 0.19 | 0.19 | 0.19 | 0.18 | 0.18 | 0.19 | mA | 0.18 | 0.19 | 0.1875 | 0 | Pass | 5 | Pass |
| Det_Current_Isc= | 0.18 | 0.18 | 0.18 | 0.18 | 0.17 | 0.17 | 0.17 | 0.17 | mA | 0.17 | 0.18 | 0.175 | 0 | Pass | 5 | Pass |
| **Test: det_range** | | | | | | | | | | | | | | | | |
| Rgood_Max= | 29 | 29 | 29 | 29 | 29 | 29 | 29 | 29 | Kohm | 29 | 29 | 29 | 26 | Pass | 32 | Pass |
| Rgood_Min= | 18 | 18 | 18 | 18 | 18 | 18 | 17 | 17 | Kohm | 17 | 18 | 17.75 | 16 | Pass | 19 | Pass |
| Rsig_det= | 29 | 29 | 29 | 29 | 29 | 29 | 29 | 29 | Kohm | 29 | 29 | 29 | 26 | Pass | 33 | Pass |
| Cgood_Max= | 0.1 | 0.1 | 0.1 | 0.1 | 0.1 | 0.1 | 0.1 | 0.1 | uF | 0.1 | 0.1 | 0.1 | 0 | Pass | 10 | Pass |
| Rbad_Cbad_Stat= | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | **** | 0 | 0 | 0 | 0 | Pass | 0 | Pass |
| **Test: det_time** | | | | | | | | | | | | | | | | |
| Backoff_Time_Tdbo= | 141 | 148 | 141 | 141 | 141 | 148 | 148 | 148 | msec | 141 | 148 | 144.5 | -1 | Pass | 16000 | Pass |
| Eff_Backoff_Tdbo_eff= | 1400 | 148 | 141 | 141 | 141 | 148 | 148 | 1400 | msec | 141 | 1400 | 458.375 | -1 | Pass | 16000 | Pass |
| Backoff_Type= | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | **** | 0 | 0 | 0 | 0 | Pass | 1 | Pass |
| Detection_Time_Tdet= | 301 | 309 | 305 | 301 | 305 | 305 | 309 | 309 | msec | 301 | 309 | 306.5 | 5 | Pass | 500 | Pass |
| Total_Det_Time= | 309 | 309 | 309 | 309 | 309 | 316 | 309 | 309 | msec | 309 | 316 | 309.875 | 5 | Pass | 1000 | Pass |
| **Test: det_resource** | | | | | | | | | | | | | | | | |
| Output_Impedance_Zout= | 369.3 | 326.5 | 342.2 | 342.2 | 326.5 | 286.2 | 342.2 | 378.1 | KOhm | 286.2 | 378.1 | 337.9 | 45 | Pass | 2000 | Pass |
| **Test: class_v** | | | | | | | | | | | | | | | | |
| Class_Voltage_Vclass= | 17.3 | 17.6 | 17.6 | 16.6 | 17.7 | 17.7 | 17.6 | 17.5 | volts | 16.6 | 17.7 | 17.45 | 15.5 | Pass | 20.5 | Pass |
| Vclass_Min= | 17.6 | 17.7 | 17.5 | 17.4 | 17.5 | 17.5 | 17.4 | 17.3 | volts | 17.3 | 17.7 | 17.4875 | 15.5 | Pass | 20.5 | Pass |
| **Test: class_time** | | | | | | | | | | | | | | | | |
| Event_Count= | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | **** | 1 | 1 | 1 | 1 | Pass | 2 | Pass |
| Class_Time_Tpdc= | 15.6 | 13.6 | 13.6 | 13.6 | 13.6 | 13.6 | 13.6 | 13.6 | msec | 13.6 | 15.6 | 13.95 | 6 | Pass | 75 | Pass |
| **Test: class_err** | | | | | | | | | | | | | | | | |
| Class_Iin= | 65 | 65 | 65 | 65 | 65 | 65 | 65 | 65 | mA | 65 | 65 | 65 | 51 | Pass | 100 | Pass |
| Vport_CL_Iin= | 14.7 | 14.9 | 14.9 | 15.1 | 15.1 | 15.1 | 14.9 | 15.1 | V | 14.7 | 15.1 | 14.975 | 0 | Pass | 20.5 | Pass |
| Vport_CL_err_1= | 17.1 | 16.9 | 17 | 17 | 17.1 | 17.1 | 16.9 | 16.9 | V | 16.9 | 17.1 | 17 | 0 | Pass | 20.5 | Pass |
| **Test: class_lldp** | | | | | | | | | | | | | | | | |
| PSE_Source_Priority= | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | * | 0 | 0 | 0 | 0 | Pass | 0 | Pass |
| PSE_MDI_Pwr_Sup= | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | * | 0 | 0 | 0 | 0 | Pass | 0 | Pass |
| PSE_LLDP_Time_2= | 2.8 | 2.7 | 2.8 | 2.4 | 2.7 | 15.6 | 2.6 | 16.7 | sec | 2.4 | 16.7 | 6.1625 | 0 | Pass | 10 | Fail |
| PSE_LLDP_Type_2= | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | * | 2 | 2 | 2 | 2 | Pass | 2 | Pass |
| PSE_Echo_Time_2= | 4 | 1.7 | 0.2 | 4 | 2.1 | 5.9 | 1.7 | 4.7 | sec | 0.2 | 5.9 | 3.0375 | 0 | Pass | 10 | Pass |
| PSE_Alloc_Pwr_2= | 20.3 | 20.3 | 20.3 | 20.3 | 20.3 | 20.3 | 20.3 | 20.3 | Watts | 20.3 | 20.3 | 20.3 | 20.3 | Pass | 25.5 | Pass |
| PSE_Alloc_Time_2= | 4 | 1.7 | 0.2 | 4 | 2.1 | 5.9 | 1.7 | 4.7 | sec | 0.2 | 5.9 | 3.0375 | 0 | Pass | 30 | Pass |
| PD_Power_Adjust_2= | 26.6 | 26.6 | 26.6 | 26.6 | 26.6 | 26.6 | 26.6 | 26.6 | Watts | 26.6 | 26.6 | 26.6 | 26.6 | Pass | 26.6 | Pass |
| PSE_Adjust_Time_2= | 2.1 | 4 | 2.1 | 2.1 | 3.6 | 3.2 | 4 | 3.2 | sec | 2.1 | 4 | 3.0375 | 0 | Pass | 10 | Pass |
| **Test: pwrup_time** | | | | | | | | | | | | | | | | |
| Pwr-On_Rise_Time_Trise= | 16 | 35 | 16 | 44 | 37 | 16 | 15 | 41 | usec | 15 | 44 | 27.5 | 15 | Pass | 50000 | Pass |
| Power-On_Time_Tpon= | 7.8 | 62.5 | 66.4 | 128.9 | 15.6 | 15.6 | 15.6 | 46.9 | msec | 7.8 | 128.9 | 44.9126 | 0 | Pass | 400 | Pass |
| **Test: pwrup_inrush** | | | | | | | | | | | | | | | | |
| Init_Inrush= | 430 | 428.63 | 428.38 | 427.75 | 428.25 | 432.25 | 429 | 428.63 | mA | 427.75 | 432.25 | 429.11125 | 400 | Pass | 512 | Pass |
| Max_Inrush_c4= | 429 | 428 | 427.13 | 426.75 | 427.25 | 431 | 428.88 | 427.5 | mA | 426.75 | 431 | 428.18875 | 400 | Pass | 450 | Pass |
| Min_Inrush= | 427 | 426.13 | 425.13 | 425.5 | 425.88 | 429.13 | 426.63 | 425.63 | mA | 425.13 | 429.13 | 426.37875 | 400 | Pass | 450 | Pass |
| Tinrush= | 59.2 | 59.2 | 59.2 | 59.2 | 59.6 | 59.6 | 59.6 | 59.6 | msec | 59.2 | 59.6 | 59.4 | 50 | Pass | 75 | Pass |
| Inrush_45m= | 54.4 | 54.1 | 54.2 | 54.2 | 54.2 | 54.3 | 54.1 | 54.3 | Volts | 54.1 | 54.4 | 54.225 | 50 | Pass | 57 | Pass |
| Inrush_Voltage= | 35.3 | 35.1 | 35.2 | 35.2 | 35.3 | 35.5 | 35.5 | 35.4 | Volts | 35.1 | 35.5 | 35.3125 | 30 | Pass | 57 | Pass |
| Max_Init_Inrush= | 714 | 713 | 713.8 | 713.3 | 713 | 714.6 | 713.3 | 714.3 | mA | 713 | 714.6 | 713.85 | 0 | Pass | 2000 | Pass |
| Inrush_Strategy= | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | **** | 0 | 0 | 0 | 0 | Pass | 0 | Pass |
| **Test: pwron_v** | | | | | | | | | | | | | | | | |
| Vport_min_2= | 53.6 | 53.4 | 53.4 | 53.4 | 53.4 | 53.6 | 53.3 | 53.5 | V | 53.3 | 53.6 | 53.45 | 50 | Pass | 57 | Pass |
| Vport_max_2= | 54.6 | 54.3 | 54.3 | 54.3 | 54.3 | 54.5 | 54.3 | 54.4 | V | 54.3 | 54.6 | 54.375 | 50 | Pass | 57 | Pass |
| Vport_ripple_2= | 6 | 6 | 6 | 6 | 7 | 6 | 6 | 6 | mVpp | 6 | 7 | 6 | 0 | Pass | 600 | Pass |
| Vport_noise_2= | 10 | 10 | 9 | 8 | 7 | 9 | 9 | 9 | mVpp | 7 | 10 | 8.875 | 0 | Pass | 200 | Pass |
| Vtrans_min_2= | 53 | 52.8 | 52.7 | 52.8 | 52.8 | 52.9 | 52.7 | 52.8 | V | 52.7 | 53 | 52.8125 | 50 | Pass | 57 | Pass |
| Vtrans_max_2= | 54.8 | 54.4 | 54.5 | 54.5 | 54.5 | 54.7 | 54.4 | 54.6 | V | 54.4 | 54.8 | 54.55 | 50 | Pass | 57 | Pass |
| **Test: pwron_pwrcap** | | | | | | | | | | | | | | | | |
| Pcon_c4= | 31.4 | 31.5 | 31.3 | 31.4 | 31.6 | 31.3 | 31.4 | 31.4 | watts | 31.3 | 31.6 | 31.4125 | 30 | Pass | 38.9 | Pass |
| Icon_c4= | 587 | 587 | 584 | 584 | 587 | 584 | 584 | 584 | mA | 584 | 587 | 585.125 | 526.3 | Pass | 683 | Pass |
| Type-2_Enable= | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | **** | 0 | 0 | 0 | 0 | Pass | 0 | Pass |
| **Test: pwron_maxi** | | | | | | | | | | | | | | | | |
| Ilim_Peak= | 362.5 | 363 | 366 | 364 | 360.8 | 367.5 | 364.5 | 369 | mA | 360.8 | 369 | 364.5375 | 0 | Pass | 1750 | Pass |
| Ilim_Min_2= | 696.8 | 695.8 | 696.5 | 695.5 | 696 | 697 | 696 | 697 | mA | 695.5 | 697 | 696.325 | 683 | Pass | 1750 | Pass |
| Tilm_2= | 61.3 | 60.5 | 60.9 | 60.9 | 62.5 | 62.1 | 61.7 | 62.1 | msec | 60.5 | 62.5 | 61.5 | 10 | Pass | 75 | Pass |
| Vilm_2= | 53.2 | 53 | 52.9 | 53 | 53 | 53.2 | 52.9 | 53 | V | 52.9 | 53.2 | 53.025 | 50 | Pass | 57 | Pass |
| Ilim_Max_2= | 861.3 | 860 | 860.8 | 860 | 860.5 | 861.5 | 860.3 | 861.5 | mA | 860 | 861.5 | 860.7375 | 0 | Pass | 1750 | Pass |
| Ilim_Low_V_Tol_2= | 59.8 | 59.4 | 60.2 | 60.2 | 59 | 60.5 | 60.5 | 59.4 | msec | 59 | 60.5 | 59.875 | 10 | Pass | 9999 | Pass |
| Rtrap_lo= | 106.4 | 106 | 105.9 | 106 | 106 | 106.3 | 105.8 | 106.1 | % | 105.8 | 106.4 | 106.0625 | 92.4 | Pass | 115 | Pass |
| **Test: pwron_overld** | | | | | | | | | | | | | | | | |
| vIpeak_2= | 125 | 125 | 125 | 125 | 125 | 125 | 125 | 125 | % | 125 | 125 | 125 | 0 | Pass | 125 | Pass |
| Vport_Ipeak_2= | 53.2 | 53 | 53 | 53 | 53 | 53.2 | 53 | 53.1 | V | 53 | 53.2 | 53.0875 | 50 | Pass | 57 | Pass |
| Vport_VDC_2= | 53.4 | 53.1 | 53 | 53.1 | 53.1 | 53.3 | 53 | 53.1 | V | 53 | 53.4 | 53.1375 | 50 | Pass | 57 | Pass |
| **Test: mps_dc_valid** | | | | | | | | | | | | | | | | |
| Min_Valid_Time_Tmps= | 10 | 10 | 10 | 10 | 10 | 10 | 10 | 10 | msec | 10 | 10 | 10 | 1 | Pass | 60 | Pass |
| Duty_Cycle_tol= | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | **** | 1 | 1 | 1 | 1 | Pass | 1 | Pass |
| **Test: mps_dc_pwrdn** | | | | | | | | | | | | | | | | |
| Min_Valid_I_hold= | 8 | 8 | 8 | 8 | 9 | 9 | 9 | 9 | mA | 8 | 9 | 8.5 | 5 | Pass | 10 | Pass |
| Time-to-Shutdown_Tmpdo= | 374 | 375 | 375 | 375 | 386 | 384 | 386 | 382 | msec | 374 | 386 | 379.5 | 300 | Pass | 400 | Pass |
| Max_Voltage_Vopen_max= | 0.8 | 0.8 | 0.8 | 0.8 | 0.9 | 0.8 | 0.8 | 0.8 | volts | 0.8 | 0.9 | 0.8125 | -1 | Pass | 30 | Pass |
| **Test: pwrdn_overld** | | | | | | | | | | | | | | | | |
| Iout_2= | 596 | 596 | 593 | 593 | 596 | 593 | 596 | 596 | mA | 593 | 596 | 594.875 | -1 | Pass | 683 | Pass |
| Tout_2= | 62.9 | 67.9 | 65.4 | 66.3 | 66.2 | 64.1 | 66 | 66.7 | msec | 62.9 | 67.9 | 65.6875 | -1 | Pass | 75 | Pass |
| Imoft_2= | -1 | -1 | -1 | -1 | -1 | -1 | -1 | -1 | mA | -1 | -1 | -1 | -1 | Pass | 683 | Pass |
| Tmoft_2= | -1 | -1 | -1 | -1 | -1 | -1 | -1 | -1 | msec | -1 | -1 | -1 | -1 | Pass | 2000 | Pass |
| **Test: pwrdn_time** | | | | | | | | | | | | | | | | |
| Turn-Off_Time_Toff= | 56.1 | 54.7 | 55.6 | 57.7 | 54 | 54.5 | 54.8 | 55.9 | mSec | 54 | 57.7 | 55.4125 | 0 | Pass | 500 | Pass |
| Output_Cap_Cout= | 0.1005 | 0.1011 | 0.1013 | 0.1058 | 0.0942 | 0.0949 | 0.0995 | 0.1007 | uF | 0.0942 | 0.1058 | 0.09975 | -1 | Pass | 0.52 | Pass |
| Output_Load_Rp= | 499.9 | 464.1 | 480.1 | 473.2 | 537.3 | 539.4 | 485.6 | 494.5 | Kohm | 464.1 | 539.4 | 496.7625 | 45 | Pass | 50000 | Pass |
| **Test: pwrdn_v** | | | | | | | | | | | | | | | | |
| Avg_Idle_Voff= | 0.5 | 0.5 | 0.5 | 0.5 | 0.5 | 0.5 | 0.5 | 0.5 | VDC | 0.5 | 0.5 | 0.5 | 0 | Pass | 2.8 | Pass |
| Error_Delay_Tedv= | 1796.9 | 2265.6 | 2304.7 | 2304.7 | 2304.7 | 2304.7 | 1328.1 | 2265.6 | msec | 1328.1 | 2304.7 | 2109.375 | 760 | Pass | 10000 | Pass |
| Peak_Error_Delay_Vedv= | 8 | 18.3 | 18.4 | 18.3 | 18.5 | 18.4 | 0.8 | 18.3 | VDC | 0.8 | 18.5 | 14.875 | 0 | Pass | 20.5 | Pass |

## Ordering Information

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