streamDSP

IP Datasheet

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Serial FPDP

for Altera and Xilinx FPGAs

Overview

Serial Front Panel Data Port is an industry standard, low-overhead, low-latency, high speed serial communications protocol. sFPDP is ideal for use in applications such as high-speed communication system backplanes, high-bandwidth remote sensor systems, signal processing, data recording, and high-bandwidth video systems. The simple and lightweight nature of the protocol makes it an attractive choice for replacement of parallel bus interconnects using serial transceiver technology. sFPDP can be used in point-to-point or loop topologies, uni-directional or bi-directional links, and easily supports different types of data with efficient data framing options.

StreamDSP is committed to performance, efficiency, and flexibility. Our sFPDP core is unique in that we support nearly all transceiver based devices from Altera and Xilinx. We're always making improvements to the core with innovative new features such as multi-lane bonding for increased bnadwidth, and we're continually updating the core to support new transceiver based devices offered by both Altera and Xilinx. Our core provides a open interface to the transceiver PHY, giving the user complete control over transceiver speed, settings and adjustments. A complete reference design is provided for several Altera and Xilinx development boards, as well as several simulation testbench scripts for Riviera and ModelSim. In addition, our testing procedure includes Altera <-> Xilinx communications to ensure compatibility.

User control and status information are provided as discrete top-level ports, or through a simple memory mapped interface compliant with Altera's Avalon-MM specification. The user data port is a data/valid/ready interface capable of back-pressure flow control, and is compliant with Altera's Avalon-ST specification. The core can be used in an Altera SOPC (System on a Programmable Chip) based system for easy access to and from processors and other components, or can be used in stand-alone mode and interface directly to custom logic.

Features

- VITA 17.1-2003 Compliant
- Conforms to FC-PH disparity rules
- Multi-lane channel bonding
- Independent data / system clock domains
- 600 Mbps to 6.375 Gbps serial rate support
- Optional flow control and CRC
- 32-bit user data interface
- Basic control/status interface
- Unidirectional and bidirectional support
- Real-time link status information
- All sFPDP frame types supported
  - Unframed data
  - Single frame data
  - Fixed size repeating frame data
  - Dynamic size repeating frame data
- All sFPDP system configurations supported
  - Basic System
  - Flow Control
  - Bidirectional Data Flow
  - Copy Mode
  - Copy/Loop Mode

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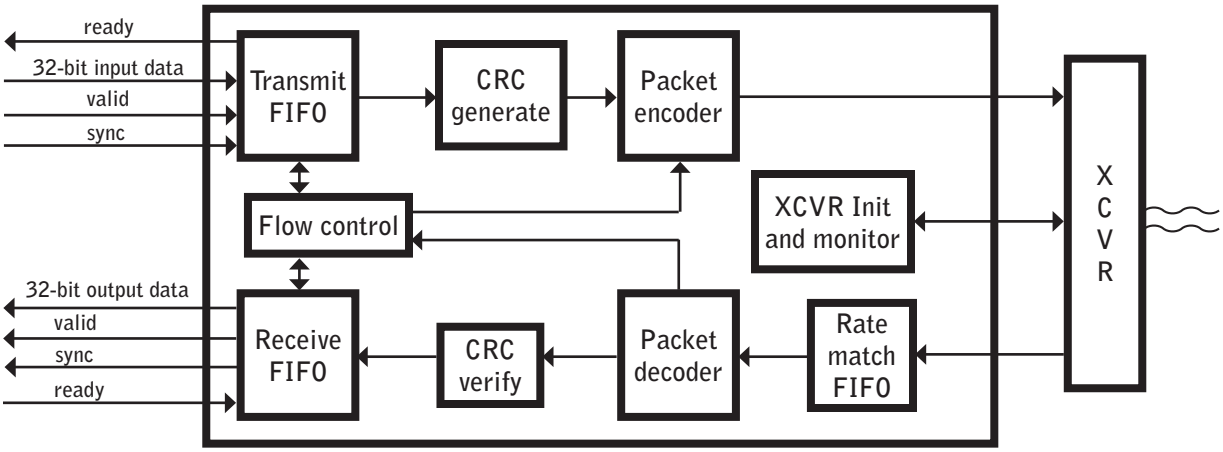
Details



Resource Usage

Flip-Flops	LUTs	RAM
772	841	14 M4K

Throughput (per lane)

Line Rate	Throughput
2.5 Gbps	247 MB/sec
4.25 Gbps	420 MB/sec
5.0 Gbps	494 MB/sec
6.375 Gbps	630 MB/sec
* 8.5 Gbps	840 MB/sec
** 10 Gbps	988 MB/sec

* 8.5G supported with Altera Stratix-IV GX in future release
** 10G supported with Altera Stratix-IV GT in future release

Additional Information

Please contact sales@streamdsp.com for additional information, including the complete IP Core User Guide and pricing information

HDL Language	VHDL
Delivery options	Encrypted source, netlist, or source code
FPGAs Supported	Altera Stratix-II GX, Stratix-IV GX Altera Arria GX, Arria-II GX Xilinx Virtex-4 FX, Virtex-5 (LXT, FXT, SXT) Xilinx Virtex-6 (LXT)
Simulation	VHDL simulation models provided Self-checking testbench scripts included for Aldec Riviera and MTI ModelSim
Dev Kit Demo's	Altera Arria GX PCI-Express Dev Kit Altera Arria-II GX PCI-Express Dev Kit Altera Stratix-II GX PCI-Express Kit Altera Stratix-IV Signal Integrity Kit Altera Stratix-IV Development Kit (PCI-E) Xilinx Virtex-4 FX ML405 board Xilinx Virtex-5 LXT ML555 board Xilinx Virtex-5 FXT ML507 board Xilinx Virtex-6 LXT ML605 board

OpenCore® Plus Support

SOPC Builder Ready

ALDEC