SYSTEM VERILOG

V1.00

One of the problems facing system designers today is that standard HDL languages such as VHDL and Verilog, while very adequate for RTL descriptions, do not have a high enough level of abstraction to describe models efficiently. They also lack the advanced verification structures that are needed with today's more complex hardware.

System Verilog is built on top of Verilog 2001. It improves the productivity, readability, and reusability of Verilog-based code. The language enhancements in System Verilog provide more concise hardware descriptions, while still providing an easy route with existing tools into current hardware implementation flows. The enhancements take on the form of programming structures that allow more robust modeling of hardware constructs, constrained randomization of data values for the creation of test vectors, and assertion-based testing. Here, the rules are established for the values of signals (related to each other) and these rules (assertions) are tested as the simulation evolves.

Level – Intermediate
Course Duration – 2 days
Price – $1600 or 16 Hardent Training Credits
Course Part Number – HDT-SYSVER-100-ILT

Who Should Attend

- HDL Designers and Verification Engineers who want to keep current with the latest trends in HDL Design Methodology. Specifically for creating more elaborate tests.

Prerequisites

- Basic HDL Language (VHDL or Verilog) knowledge

Software Tools

- ModelSim

Hardware

- None

Acquired Skills:

- A knowledge of the syntax and usage of System Verilog and how it fits into the HDL design cycle

Day 1

- Advanced Data Types (2-value vs. 4-value logic, Packed & Unpacked Arrays, Structures & Unions, Enumerated Data Types, Queues)
- System Verilog (Definitions, Inheritance)
- Associative Arrays (Inserting vs. Extracting values)
- **Lab 1 – Comparison of HDL and System Verilog**
- **Lab 2 – System Verilog Classes**

Day 2

- Random Data Generation (Generating Random Numbers, Random Constraints)
- Assertions (Immediate vs. Concurrent)
- Basic Interfaces
- Synthesis of System Verilog Structures
- **Lab 3 – Constrained Randomization**
- **Lab 4 – Assertions**

Register Today

Hardent is pleased to offer new courses to help designers produce fast, predictable and efficient designs. For a detailed list, visit www.hardent.com/training or contact Hardent's Training Coordinator for more information, to register for a class or to schedule a private course.

Email: training@hardent.com
Telephone: **514-999-3880**