Dual 250 MSPS, 14-bit ADC and Virtex-5 FPGA Processing Module

VPX-1131

Preliminary

3U VPX

Product Overview

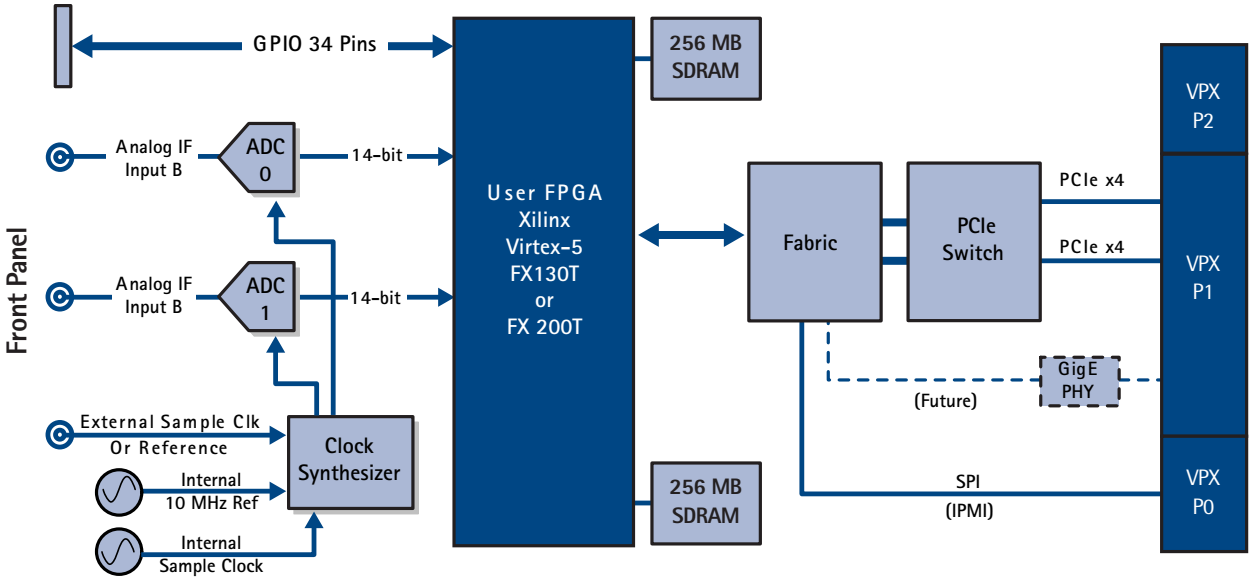
The VPX-1131 is a high-speed analog-to-digital conversion and processing module. This rugged, deployable module is equipped with a large user-programmable FPGA, tightly coupled with fast ADCs.

Features

- Dual 250 MSPS, 14-bit ADC
- 512 MB DDR2 SDRAM
- Xilinx Virtex-5 FX130T or FX200T User FPGA
- On-board clock for 200 MSPS sampling rate (other sampling rates available)
- Internal or External sample clock or External 10 MHz Reference
- 34-pin General Purpose I/O (LVTTL, LVDS) via front panel
- Multi-board synchronization for phase coherent sampling
- Two PCI Express x4 ports to VPX high-speed serial backplane
- Ruggedized conduction-cooled or air-cooled
- 3U OpenVPX (VITA 65) form factor
- Drivers and SDK, FPGA interface libraries, and example code included
- Not subject to US ITAR control

Applications

- Signals Intelligence (SIGINT)
- Communications Intelligence (COMINT)
- Electronic Support Measures (ESM)
- Electronic Countermeasures (ECM)
- Software Defined Radio and Military Communications (MILCOM)



VPX-1131 Block Diagram

Specifications

[general]	Form Factor	3U OpenVPX (Vita 65) Module
	FPGA Device	A single user-programmable Xilinx Virtex-5 FX130T or FX200T
[analog input]	A/D Converter	One Texas Instruments dual channel ADS62P49 14-bit @ 200 MHz @ up to 250 MHz
	ADC Input	AC coupled, full scale 2 Vpp into a 50 ohm load, single ended 3dB input bandwidth: 250 kHz – 190 MHz
	ADC SFDR	@ 200 MSPS, -1dBFS input: 10.7 MHz IF (10 MHz BW) > 85 dB typical 21.4 MHz IF (20 MHz BW) > 85 dB typical 70 MHz IF (30 MHz BW) > 70 dB typical 160 MHz IF (70 MHz BW) > 70 dB typical
[external interfaces]	Analog IF Input/Output,	SMA Socket 50 ohms
	External Sampling Clock	SMA Socket 50 ohms, 40 to 250 MHz, 0.75 to 1.6 Vpp
	or 10 MHz Reference	Nominally 10 MHz reference, 0.75 - 1.6 Vpp
	Host Interface	Two PCIe x4 Gen 2.0 Ports
	JTAG Connection	JTAG connector for Virtex-4/5 FPGA, Xilinx ChipScope™ debugger compatible
	General Purpose I/O (GPIO)	34 pins: 15 differential pairs & 4 single-ended
[compatibility]	Host SBC	Intel i7-based SBC with Linux drivers provided
	Operating System	Linux Red Hat 5.3 on host SBC
[development software]	Application Libraries	*quic*Comm Software Development Kit
	FPGA Code Development	ISE Foundation tools from Xilinx are required, Synplify Synthesis® from Synopsys is recommended
	HDL coding language	VHDL
	Software & FPGA Code	Examples showing dataflow from ADC to host SBC at high data rate
[electrical]	Supply Voltage (DC)	Supply Voltage +5V, 3.3V +5%/-3% (supplied by VPX connector)
	Power Consumption	30 W typical
[environmental]	Temperature	Air-cooling operating temperature range of 0 to 50 degrees C, forced air @ 600 LFM
	RoHS	5 of 6 compliant (Pb solder exemption).
[compatible modules]	VPX-2131	Dual DAC & FPGA Module
[future options]	Sample Clock	Alternate VCXO frequencies to support other sampling rates
	Alternate I/O	DC coupled analog inputs
	Additional Modules	VPX-8311 Dual DSP Module VPX-3321 Dual Transceiver Module
	Cooling	Conduction-cooled module
	Operating System	Windows 7 (on host SBC)
	SDRAM Memory	1 GB
	Gigabit Ethernet	2 ports via P1 VPX Connector

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