Dual 300 MSPS, 14-bit DAC and Virtex-5 FPGA Processing Module

VPX-2131

Preliminary

3U VPX

Product Overview

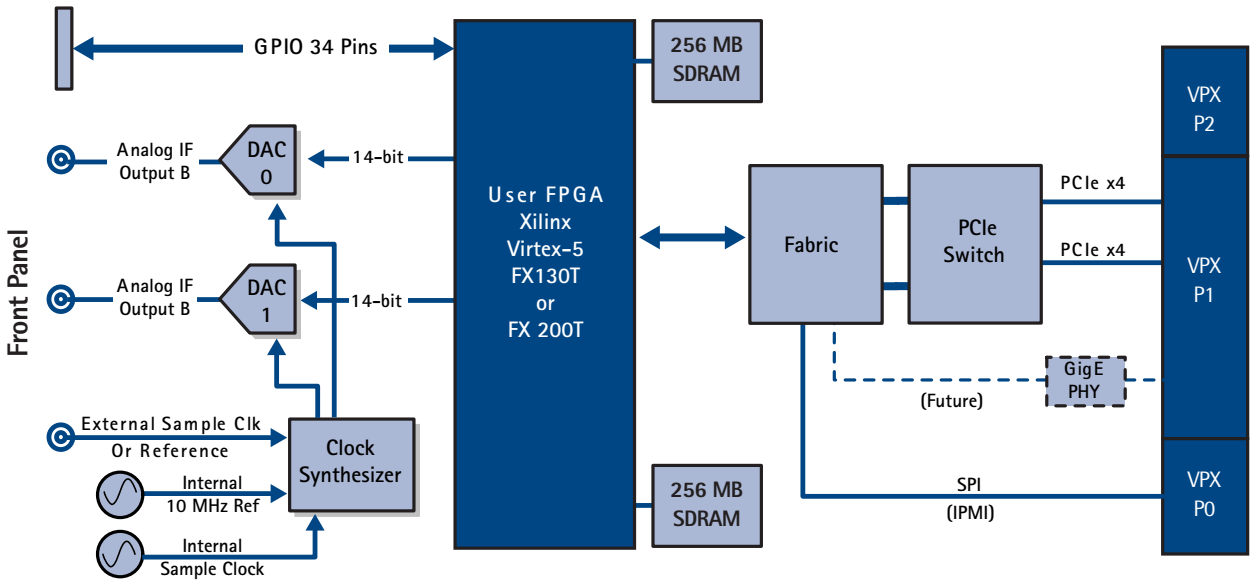
The VPX-2131 is a high-speed digital-to-analog conversion and processing module. This rugged, deployable module is equipped with a large user-programmable FPGA, tightly coupled with fast DACs.

Features

- Two 300 MSPS, 14-bit DACs
- 512 MB DDR2 SDRAM
- Xilinx Virtex-5 FX130T or FX200T User FPGA
- On-board clock supports sampling at 300 MSPS
- Internal or External Sample clock or External 10 MHz Reference
- 34-pin General Purpose I/O (LVTTL, LVDS) via front panel
- Multi-board synchronization for phase coherent sampling
- Two PCI Express x4 ports to VPX high-speed serial backplane
- Ruggedized conduction-cooled or air-cooled
- 3U OpenVPX (VITA 65) form factor
- Drivers and SDK, FPGA interface libraries, and example code included
- Not subject to US ITAR control

Applications

- Electronic Countermeasures (ECM)
- Electronic Support Measures (ESM)
- Software Defined Radio and Military Communications (MILCOM)
- Signals Intelligence (SIGINT)
- Communications Intelligence (COMINT)



VPX-2131 Block Diagram

Specifications

[general]	Form Factor	3U OpenVPX (VITA 65) Module
	FPGA Device	A single user-programmable Xilinx Virtex-5 FX130T or FX200T
[analog output]	D/A Converter	Two Analog Devices AD9755 14-bit @ 300 MSPS @ up to 300 MHz Standard product is equipped with a 600 MHz VCSO for sampling at 300 MSPS on the internal clock
	DAC Output	AC coupled, max of 0.61 Vpp into a 50 ohm load when driven at +/- full scale 3 dB output bandwidth: 500 kHz-190 MHz (corrected for DAC sinc function)
	DAC SFDR	@300 MSPS, single tone -1 dBFS 10.7 MHz IF (10 MHz BW) > 80 dB typical 21.4 MHz IF (20 MHz BW) > 75 dB typical 70 MHz IF (20 MHz BW) > 75 dB typical @210 MSPS, single tone -1 dBFS 70 MHz IF (30 MHz BW) > 80 dB typical
[external interfaces]	Analog IF Input/Output,	SMA Socket 50 ohms
	External Sampling Clock	SMA Socket 50 ohms, 110 to 300 MHz, 0.75 - 1.6 Vpp
	or 10 MHz Reference	Nominally 10 MHz reference, 0.75 - 1.6 Vpp
	Host Interface	Two PCIe x4 Gen 2.0 Ports
	JTAG Connection	JTAG connector for Virtex-4/5 FPGA, Xilinx ChipScope™ debugger compatible
	General Purpose I/O (GPIO)	34 pins: 15 LVDS pairs & 4 single-ended
[compatibility]	Host SBC	Intel i7-based SBC with Linux drivers provided
	Operating System	Linux Red Hat 5.3 on host SBC
[development software]	Application Libraries	*quic*Comm Software Development Kit
	FPGA Code Development	ISE Foundation tools from Xilinx are required, Synplify Synthesis® from Synopsys is recommended
	HDL coding language	VHDL
	Software & FPGA Code	Examples showing dataflow from Host SBC to DAC
[electrical]	Supply Voltage (DC)	Supply Voltage +5V, 3.3V +5%/-3% (supplied by VPX connector)
	Power Consumption	30 W typical
[environmental]	Temperature	Air-cooling operating temperature range of 0 to 50 degrees C, forced air @ 600 LFM
	RoHS	5 of 6 compliant (Pb solder exemption).
[compatible modules]	VPX-1131	Dual ADC & FPGA Module
[future options]	Sample Clock	Alternate VCXO frequencies to support other sampling rates
	Alternate I/O	DC coupled analog outputs
	Additional Modules	VPX-8311 Dual DSP Module VPX-3321 Dual Transceiver Module
	Cooling	Conduction Cooled
	Operating System	Windows 7 (on host SBC)
	SDRAM Memory	1 GB
	Gigabit Ethernet	2 ports via P1 VPX Connector

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