Essential Design with the PlanAhead Analysis and DesignTool

FPGA 2

FPGA12000-13-ILT (v1.0H)

Course Specification

Course Description

Learn to manage design performance, plan an I/O pin layout, and implement by using the PlanAhead™ software tool. Topics include: a tool overview, running a Design Rule Check (DRC) and Simultaneous Switching Noise (SSN) analysis of pin assignments, design and timing analysis, creating cores, and completing synthesis and implementation with the PlanAhead tool.

Note: The hands-on labs provided within this course are identical to the tutorials that are packaged with the PlanAhead tool. This course is supplemented with instructor-led presentations and a demonstration.

Level – FPGA 2

Course Duration – 1 day

Price – $700 or 7 Training Credits

Course Part Number – FPGA12000-13-ILT

Who Should Attend? – FPGA designers, system architects, and system engineers who are interested in analyzing and driving the physical implementation of their designs to maximize performance and capacity.

Prerequisites

- *Essentials of FPGA Design* or equivalent knowledge of the FPGA architecture and the Xilinx ISE® software flow
- *Designing for Performance* recommended

Software Tools

- Xilinx ISE Design Suite: Logic or System Edition 13.1

Hardware

- Architecture: Virtex®-6 FPGA*
- Demo board: None*

* This course focuses on the Virtex-6 architecture. Check with your local Authorized Training Provider for specifics or other customizations.

After completing this comprehensive training, you will have the necessary skills to:

- Use the PlanAhead software features and benefits
- Import designs into the PlanAhead software project environment
- Assign I/O pins for optimum speed
- Run the Design Rule Checker (DRC) and perform noise analysis
- Import HDL sources and elaborate and analyze RTL netlists
- Implement the design with different implementation strategies
- Instantiate a core from the Xilinx IP Catalog
- Take advantage of the ISim simulator
- Use the PlanAhead software integrated with the ISE Project Navigator software environment

Course Outline

- PlanAhead Software Benefits and Features Overview
- PlanAhead Software Project Manager
- **Lab 1:** Getting Started with the PlanAhead Software
- I/O Pin Planning
- **Lab 2:** Assigning I/O Pins
- CORE Generator Software Integration
- **Lab 3:** Core Integration
- Static Timing Analysis with the PlanAhead Software
- Project Navigator Integration with the PlanAhead Software
- Introduction to the *Advanced Design with the PlanAhead Analysis and Design Tool* Course

Lab Descriptions

Note: All labs within this course are also available as self-guided tutorials, which are packaged with the PlanAhead tool.

- **Lab 1:** Getting Started with the PlanAhead Software – Illustrates the steps you take to import an RTL design into the PlanAhead software so that you can synthesize, implement, perform timing analysis, view logical and device resources, and generate a bitstream. Also introduces the PlanAhead software's environment and views.
- **Lab 2:** Assigning I/O Pins – Introduces the PlanAhead software's pin planning environment for performing I/O pin assignment. You will create a pin planning project, import and export I/O ports lists, create I/O ports and interfaces, run a DRC and SSN noise analysis, examine clock logic placement, and make pin assignments.
- **Lab 3:** CORE Integration – Illustrates the integration of the CORE Generator software with the PlanAhead software. You will customize and integrate a core, explore the IP Catalog, and view the generated core with the Schematic viewer.

Register Today

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