Course Description

Learn to increase design performance and achieve repeatable performance by using the PlanAhead™ software tool. Topics include: synthesis and project tips, design analysis, creating a floorplan, improving performance with area constraints and Pblocks, design debugging with the ChipScope™ Pro tool, and design preservation with partitions.

Note: The hands-on labs provided within this course are identical to the tutorials that are packaged with the PlanAhead tool. This course is supplemented with instructor-led presentations and demonstrations.

Level – FPGA 3
Course Duration – 2 days
Price – $1200 or12 Xilinx Training Credits
Course Part Number – FPGA22000-13-ILT
Who Should Attend? – FPGA designers, system architects, and system engineers who are interested in analyzing and driving the physical implementation of their designs to maximize performance and capacity.
Prerequisites
- *Essentials of FPGA Design* or equivalent knowledge of the FPGA architecture and the Xilinx ISE® software flow
- *Essential Design with the PlanAhead Analysis and Design Tool* or equivalent knowledge of the PlanAhead software
- *Designing for Performance* recommended

Software Tools
- Xilinx ISE Design Suite: Logic or System Edition 13.1

Hardware
- Architecture: Virtex®-6 FPGA*
- Demo board: None*

* This course focuses on the Virtex-6 architecture. Check with your local Authorized Training Provider for for specifics or other customizations.

After completing this comprehensive training, you will have the necessary skills to:
- Use the most advanced features of the PlanAhead software
- Apply the hierarchical viewer and timing report information to make the best area constraints
- Group the best logic into Pblocks
- Import HDL sources, elaborate, and analyze an RTL netlist
- Implement the design with different implementation strategies
- Analyze design statistics, connectivity, timing, placement, and timing critical paths
- Insert ChipScope Pro tool debug cores
- Floorplan the design to improve performance and preserve successful implementation results
- Make placement constraints for dedicated hardware resources

Course Outline
Day 1
- PlanAhead Software Review
- **Lab 1:** PlanAhead Software Review
- RTL Development and Analysis
- **Lab 2:** RTL Analysis
- Placing Dedicated Resources
- **Lab 3:** Placing Dedicated Resources
- Introduction to Pblocks
- Floorplanning Techniques

Day 2
- Floorplanning Case Studies
- **Lab 4:** Design Analysis and Floorplanning for Performance
- Design Preservation with Partitions
- **Lab 5:** Leveraging Design Preservation for Predictable Results
- Debugging with the ChipScope Pro Tool
- **Lab 6:** Debugging with the ChipScope Tool
- Tcl Scripting in the PlanAhead Software
- **Lab 7:** Tcl Commands
- (Optional): Team Design
- (Optional): Routing Optimization in Virtex-6 Devices

Lab Descriptions
Note: All labs within this course are also available as self-guided tutorials, which are packaged with the PlanAhead tool.
- **Lab 1:** PlanAhead Software Review – Illustrates the steps you take to import source HDL files into the PlanAhead tool and synthesize, implement, and analyze the results. Also introduces the PlanAhead tool environment and views.
- **Lab 2:** RTL Analysis – Provides an overview of the RTL development and analysis environment. You will analyze the RTL logic hierarchy, RTL schematic, RTL resource estimations, RTL power estimations, and run an RTL Design Rule Check (DRC).
- **Lab 3:** Placing Dedicated Resources – Introduces the methods for assigning location constraints to dedicated hardware resources. Demonstrates how to assign dedicated clocking resources, work with multi-function I/O pins, and complete a SSN noise analysis.
- **Lab 4:** Design Analysis and Floorplanning for Performance – Introduces the pre- and post-implementation design analysis features of the PlanAhead software. Provides an introduction to some of the capabilities and benefits of using the PlanAhead tool for designing high-end FPGAs.
- **Lab 5:** Leveraging Design Preservation for Predictable Results – Introduces the use of partitions to maintain successful implementation results.
- **Lab 6:** Debugging with the ChipScope Tool – Provides an introduction to using the PlanAhead tool for debugging designs with the ChipScope Pro tool, cores, and Set Up ChipScope Wizard.
- **Lab 7:** Tcl Commands – Use the Tcl interface in the PlanAhead software.

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