Introduction to the Zynq EPP Architecture

Embedded Hardware and Firmware 3

EMBD24010-14-ILT (v1.0H)

Course Specification

Course Description

This course provides hardware and firmware engineers with the knowledge to effectively utilize a Zynq™ EPP system on a chip. It covers the architecture of the ARM® Cortex™-A9 processor-based processing system (PS) and the integration of programmable logic (PL).

The course also details the individual components that comprise the PS, I/O peripherals, timers, and caching, as well as the DMA, interrupt, and memory controllers. Emphasis will be placed on effective access and usage of the PS DDR controller from PL user logic, efficient PL-to-PS interfacing, and design techniques.

Level – Embedded Hardware and Firmware 3

Course Duration – 1 day

Price – $800 or 8 Training Credits

Course Part Number – EMBD24010-14-ILT

Who Should Attend? – Hardware and firmware engineers who are interested in implementing a system on a chip using the Zynq EPP and programmable logic.

Prerequisites

- FPGA design experience
- Completion of the *Essentials of FPGA Design* course or equivalent knowledge of Xilinx ISE® software implementation tools
- Basic understanding of C programming
- Basic understanding of microprocessors
- Some HDL modeling experience

Software Tools

- Xilinx ISE Design Suite: Embedded or System Edition 14.1

Hardware

- Architecture: Zynq-7000 EPP*
- Demo board: Zynq-7000 EPP ZC702 demo board*

* This course focuses on the Zynq-7000 EPP. Check with Hardent for the specifics of the in-class lab board or other customizations.

After completing this comprehensive training, you will have the necessary skills to:

- Describe the architecture and components that comprise the Zynq EPP processing system (PS)
- Evaluate a processing system (PS) and programmable logic (PL) AXI interface
- Identify the configuration options for the Zynq EPP

Course Outline

- Zynq EPP Architecture Overview
- Inside the Application Processor Unit (APU)
- Processor Input/Output Peripherals
- **Lab 1:** Building a Zynq Extensible Processing Platform
- Zynq System Architecture Essentials
- Zynq EPP PS/PL AXI Ports
- **Lab 2:** Integrating Programmable Logic on the Zynq EPP
- Zynq Device Configuration
- Zynq EPP Memory Resources
- **Lab 3:** Running and Debugging a Linux Application on the Zynq EPP

Lab Descriptions

- **Lab 1:** Building a Zynq Extensible Processing Platform – Examine the process of using the PlanAhead™ and Xilinx Platform Studio (XPS) tools to create a simple processing system.
- **Lab 2:** Using DMA on the Zynq EPP – Experiment with effectively using the PS DMA controller to move data between DDRx memory and a custom PL peripheral.
- **Lab 3:** Running Linux on the Zynq EPP – Explore a software application executing under the Linux operating system on the Zynq EPP.

Register Today

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