Zynq EPP System Architecture

Embedded Architect 3

EMBD24000-14-ILT (v1.0H)

Course Specification

Course Description

The Xilinx Zynq™ Extensible Processing Platform (EPP) provides a new level of system design capabilities. This course provides experienced system architects with the knowledge to effectively architect a Zynq EPP system on a chip.

This course presents the features and benefits of the Zynq architecture for making decisions on architecting a Zynq EPP project. It covers the architecture of the ARM® Cortex™-A9 processor-based processing system (PS) and the integration of programmable logic (PL) at a sufficiently deep level that a system designer can successfully and effectively utilize the Zynq EPP.

The course also details the individual components that comprise the PS, I/O peripherals, timers, and caching, as well as the DMA, interrupt, and memory controllers. Emphasis will be placed on effective access and usage of the PS DDR controller from PL user logic, efficient PL-to-PS interfacing, and design techniques, tradeoffs, and advantages of implementing functions in the PS or the PL.

Level – Embedded Architect 3

Course Duration – 2 days

Price – $1500 0r 15 Training Credits

Course Part Number – EMBD24000-14-ILT

Who Should Attend? – System architects who are interested in architecting a system on a chip using the Zynq EPP.

Prerequisites

- Digital system architecture design experience
- Basic understanding of microprocessor architecture
- Basic understanding of C programming
- Basic HDL modeling experience

Software Tools

- Xilinx ISE Design Suite: Embedded or System Edition 14.1

Hardware

- Architecture: Zynq-7000 EPP*
- Demo board: Zynq-7000 EPP ZC702 demo board*

* This course focuses on the Zynq-7000 EPP. Check with Hardent for the specifics of the in-class lab board or other customizations.

After completing this comprehensive training, you will have the necessary skills to:

- Describe the architecture and components that comprise the Zynq EPP processing system (PS)
- Relate a user design goal to the function, benefit, and use of the Zynq EPP
- Effectively select and design an interface between the Zynq PS and programmable logic (PL) that meets project goals
- Analyze the tradeoffs and advantages of performing a function in software versus PL

Course Outline

Day 1

- Zynq EPP Architecture Overview
- Inside the Application Processor Unit (APU)
- Processor Input/Output Peripherals
- **Lab 1:** Building a Zynq Extensible Processing Platform
- Zynq System Architecture Essentials
- Introduction to AXI
- Zynq EPP PS/PL AXI Ports
- **Lab 2:** Integrating Programmable Logic on the Zynq EPP

Day 2

- Zynq Device Configuration
- Zynq EPP Memory Resources
- Zynq EPP PL Design Architecture
- Meeting Your Performance Goals
- **Lab 3:** Using DMA on the Zynq EPP
- Zynq EPP Software Design
- Debugging the Zynq EPP
- **Lab 4:** Debugging on the EPP
- Zynq EPP Tools and Reference Designs
- **Lab 5:** Running Linux on the Zynq EPP

Lab Descriptions

- **Lab 1:** Building a Zynq Extensible Processing Platform – Examine the process of using the PlanAhead™ and Xilinx Platform Studio (XPS) tools to create a simple processing system.
- **Lab 2:** Integrating Programmable Logic on the Zynq EPP – Connect a programmable logic (PL) design to the embedded processing system (PS).
- **Lab 3:** Using DMA on the Zynq EPP – Experiment with effectively using the PS DMA controller to move data between DDRx memory and a custom PL peripheral.
- **Lab 4:** Debugging on the Zynq EPP – Evaluate debugging the hardware and software components of a Zynq EPP design.
- **Lab 5:** Running Linux on the Zynq EPP – Explore a software application executing under the Linux operating system on the Zynq EPP.

Register Today

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