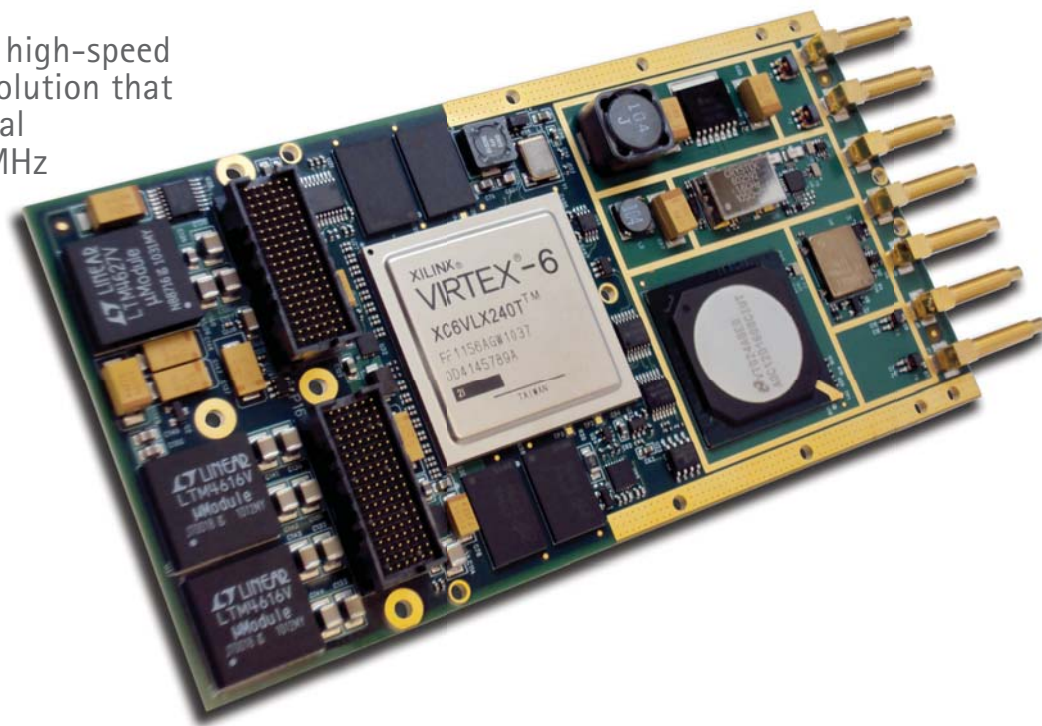


# Wideband Digital Receiver/Digitizer Module

## XMC-1151

### Product Overview

The XMC-1151 is an ultra high-speed digitizer and processing solution that enables direct RF-to-Digital conversion between 100 MHz and 3 GHz.

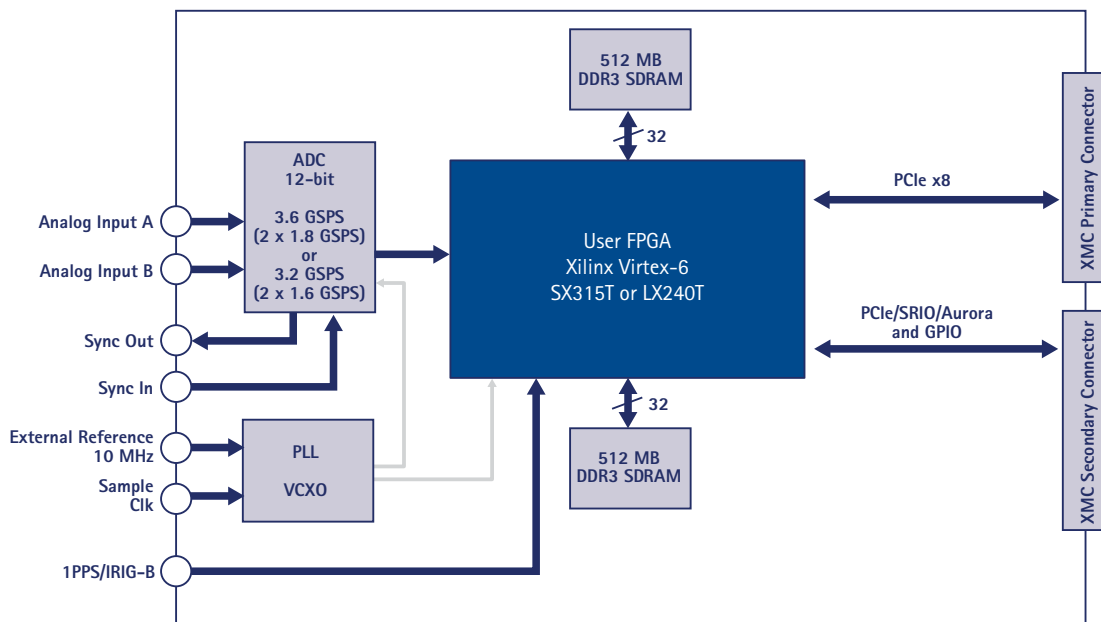


### Features

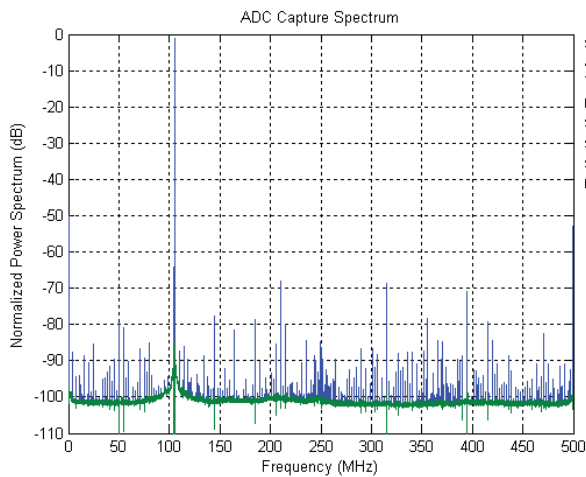
- One 3.6 GSPS 12-bit ADC channel (or two channels at 1.8 GSPS); or One 3.2 GSPS 12-bit ADC channel (or two channels at 1.6 GSPS)
- ADC analog input bandwidth up to 2.8 GHz enables bandpass sampling (Second Nyquist zone)
- Xilinx Virtex-6 SX315T or LX240T User FPGA
- 1 GB DDR3 SDRAM (2 banks of 512 MB, 1066 Mbps)
- XMC module supporting PCI Express x8 Gen 2 (VITA 42.3) (4 GB/s full-duplex)
- Supports multi-board synchronization
- Support for phase coherent sampling
- General purpose digital I/O including high speed serial
- Drivers and SDK, API, FPGA interfaces included
- Digital downconverter (DDC) IP available
- Air-cooled, rugged conduction-cooled available

### Applications

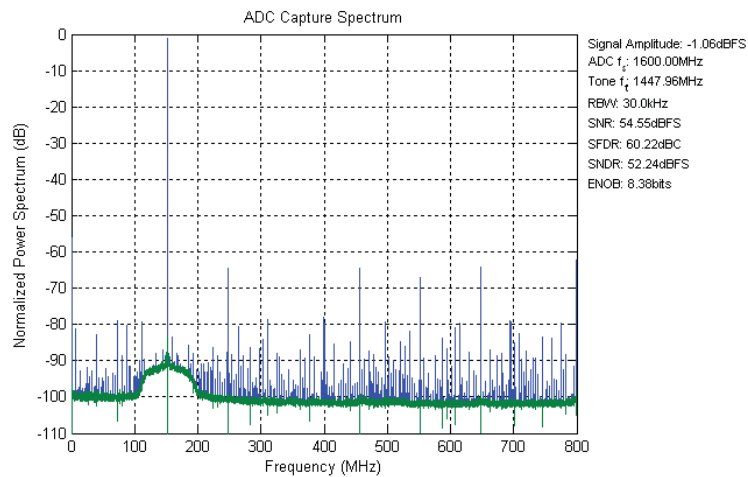
- SIGINT (COMINT/ELINT)
- RADAR
- Satellite Receiver
- Electronic Support Measures (ESM)
- Spectral Analysis
- Wideband Signal Recorder
- Software Defined Radio (SDR)
- High-Speed Test and Measurement
- Set-Top Box Development
- Wideband Sensing for Cognitive Radio
- Channel Measurement and Characterization



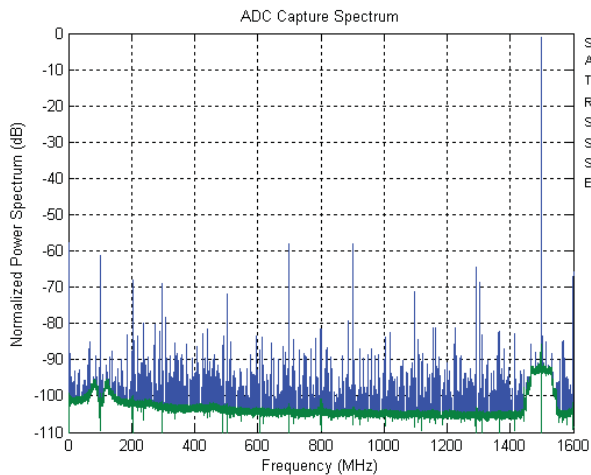
XMC-1151 Block Diagram



Sample spectral plot for 895 MHz input signal at 1.0 GSPS



Sample spectral plot for 1448 MHz input signal at 1.6 GSPS



Sample spectral plot for 1498 MHz input signal at 3.2 GSPS

## Specifications

[ general ]	Form Factor	XMC (VITA 42.3)		
	User Programmable FPGA	Xilinx Virtex-6 SX315T-2 or LX240T-2 (LX130T, LX195T, LX365T, SX475T are available as options)		
	Memory	1GB DDR3 SDRAM (2 banks of 512 MB each, 1066 Mbps)		
	Sample Clock	Internal 1.6 GHz VCSO (contact Spectrum for other frequencies) or external sample clock input		
	Reference Clock	Internal 10 MHz clock reference (+/- 2.0 ppm) or external reference input		
[ analog I/O ]	A/D Converter	Texas Instruments ADC12D1800 12-bit at 3.6 GSPS single channel or dual channel at 1.8 GSPS; or ADC12D1600 12-bit at 3.2 GSPS single channel or dual channel at 1.6 GSPS		
	ADC Input	AC coupled, single-ended Full scale input: 0 dBm 50 ohms typical Analog full power bandwidth: 5 MHz to 2.8 GHz (AC coupled)		
	ADC Characterization (typical)	895 MHz Fin with 1.0 GSPS	1448 MHz Fin with 1.6 GSPS	1498 MHz Fin with 3.2 GSPS
		ADC SFDR = 67.0 dBc	ADC SFDR = 60.2 dBc	ADC SFDR = 54.8 dBc
		ADC SNR = 58.6 dBFS	ADC SNR = 54.5 dBFS	ADC SNR = 54.3 dBFS
ADC ENOB = 9.1 Bits		ADC ENOB = 8.4 Bits	ADC ENOB = 7.9 Bits	
[ external interfaces ]	Analog Input	SSMC 50 ohms, 0 dBm typical		
	External Reference Clock	SSMC 50 ohms, 0.75 - 1.6 V <sub>pp</sub> 10 MHz clock reference		
	External Sampling Clock	SSMC 50 ohms, -3 dBm typical		
	GPS Timing Reference	SSMC 50 ohms, 1PPS/IRIG-B TTL/LVTTL		
	Sync Input/Output	Twinax 100 ohms differential connector		
	XMC Interface	PCIe Gen2 x8 link, providing 4 GB/s (full-duplex) bandwidth to XMC primary connector Configurable connection to XMC secondary connector GPIO (1 pair LVDS clock with 16 pairs LVDS data and 4 single-ended LVTTTL) plus PCIe Gen2 x8 (can be configured for SRIO or Aurora*)		
	JTAG Connection	JTAG connector for Virtex-6 FPGA, Xilinx Chipscope debugger compatible		
[ compatibility ]	Supported Carriers	PC Desktop/Server: XMC-to-PCIe Carrier Board 3U VPX: XMC-to-VPX Carrier Board AMC: XMC-to-AMC Carrier Board (single width, full height) Contact Spectrum for other compatible carriers		
	Supported Host OS	Red Hat Linux on processor card		
[ development software ]	Application Libraries	quicComm Software Development Kit		
	Multi-board Sync	Firmware to support phase coherent sampling		
	FPGA Code Development	Support for ISE Foundation tools from Xilinx or Synplify-Pro from Synopsys, Simulink/System Generator, ModelSim PE from Mentor Graphics		
	HDL Coding Language	VHDL or Verilog		
[ electrical ]	Supply Voltage (DC)	+3.3V, VPWR (5V/12V)		
	Power estimate	20W (typical)		
[ environmental ]	Operating Temperature	Air-cooled: range of 0 to 55 C, forced air at 600 LFM Industrial conduction cooled -40 to 70 C card edge		
	Shock and Vibration	Conduction cooled version VITA-47 level CC3 tested in accordance with MIL-STD-810F		
	Humidity	5-95% non-condensing. Contact Spectrum for higher ranges.		
	RoHS	5/6 compliant (Pb solder exemption)		
	MTBF	692,000 hours (GB, GC, 30 deg C), per MIL-HDBK-217 FN2 Parts Count method, Relex v8.0.		
[ ordering information ]		For VPX and AMC variations, please see the respective VPX-1151 and AMC-1151 datasheets. Stand alone modules:		
	600-00667	XMC-1151-CAC-V6SX315T-2C 12b 3.6 GSPS 1GB SDRAM		
	600-00662	XMC-1151-CAC-V6SX315T-2C 12b 3.2 GSPS 1GB SDRAM		
	600-05017	XMC-1151-CAC-V6LX240T-2 12b 3.6 GSPS 1GB SDRAM		
	600-05016	XMC-1151-CAC-V6LX240T-2 12b 3.2 GSPS 1GB SDRAM Module with PC carrier:		
	650-00626	XMC-1151-CAC-V6SX315T-2C for PC with PCIe carrier Quickstart Kit: includes a PC or VPX carrier, software and documentation to enable you to commence your development work immediately.		
	800-00535	XMC-1151-CAC-V6SX315T-2C Quickstart Kit for PC		
	800-00534	XMC-1151-CAC-V6LX240T-2 Quickstart Kit for PC		
	800-00538	AMC-1151-CAC-V6LX240T-2 Quickstart Kit for uTCA/ATCA +Red Hat Linux		
	[ future options** ]	A/D Conversion	12-bit at 2.0 GSPS single channel or dual channel at 1.0 GPSPS 12-bit at 1.0 GSPS single channel or dual channel at 500 MSPS	
Memory		2 GB DDR3 SDRAM (2 x 1 GB banks)		
ADC input		DC coupled		
*SRIO/Aurora		Software and FPGA support		
Operating System		VxWorks, Windows, INTEGRITY		

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