Quantum Channel Designer®

Addressing the Multi-Gigabit Serial Link Design & Analysis Challenge

⫶⫶⫶ SiSoft™

We Are Signal Integrity

- **Most Certified IBIS-AMI Models & Kits**
- **Broadest Correlation**
- **Automated Standards Compliance**
- **Intuitive, Superior Use Model**

Pre-Route Design Space Exploration

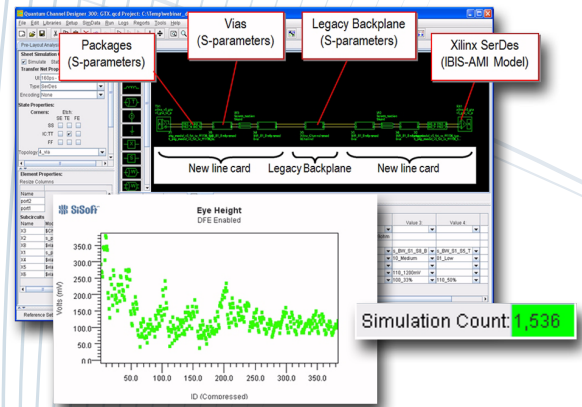**DESIGN VISION AWARD • 2009 • WINNER**

Take the guesswork out of serial link design with **Quantum Channel Designer** (QCD) – SiSoft's design and analysis environment for high-speed serial links. Its intuitive, graphical interface lets you capture, simulate and evaluate a wide range of tradeoffs to optimize your serial link for cost, performance, reliability and compliance with design standards. QCD combines advanced modeling, simulation and statistical analysis techniques with a high degree of automation to let you focus on the task at hand – evaluating design tradeoffs at all stages of your development process. QCD is the first dedicated serial link analysis tool designed for **both** system designers and signal integrity specialists.

Statistical and Time-Domain Simulation
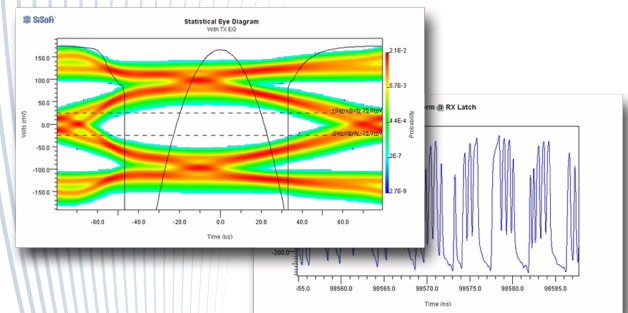
SIMULATE YOUR SERIAL CHANNEL AND SERDES IP

QCD simulates end-to-end link behavior, including **both** the passive channel and SerDes transceiver equalization / clock recovery. Evaluate how your SerDes transceivers compensate for loss, reflections and crosstalk in the channel. Determine how you can reduce system interconnect costs **without** sacrificing reliability, or assess how new SerDes transceivers can boost the performance of a legacy backplane. Quantum Channel Designer uses IBIS-AMI standard models, allowing you to simulate the unique capabilities of each vendor's technology.

Pre-route Design Space Exploration lets you sweep key design variables to identify their impact on voltage and timing margins, co-optimizing your channel design and SerDes configuration to meet performance, cost, and reliability goals. Real-time Post-Route Validation lets you analyze an entire system overnight to identify best/worst case channels and potential performance issues.
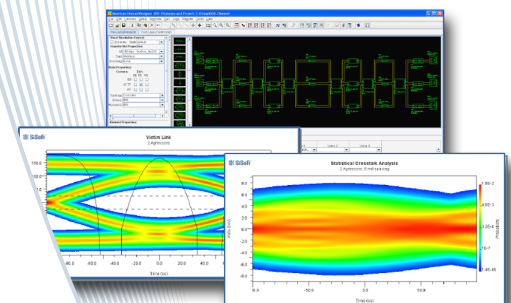
QCD's different simulation modes allow you to trade off simulation speed versus accuracy. Use statistical simulation to run thousands of simulations within minutes, identifying cases that need detailed analysis. Throughout the process, QCD reports key design metrics (i.e. insertion loss, eye height, BER or compliance to a design standard) that make it easy to compare alternatives and track trends as your design progresses.
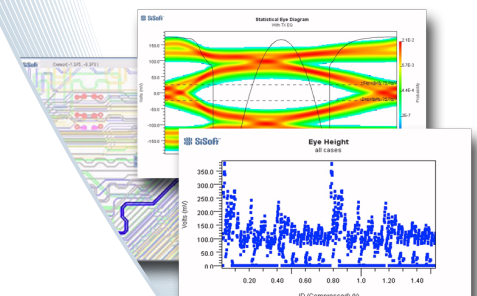

Integrated Crosstalk Analysis

Real-Time Post-Route Validation

SUPERIOR USE MODEL WITH QCD DESIGN KITS

Quantum Channel Designer accelerates your design cycle by combining advanced design kits with automated analysis:

- QCD Design Kits provide ready-to-run simulation setups for a specific vendor's technology. Determine margins for your design by importing your channel model and running simulation - a process that **takes less than 2 minutes**.

- QCD's structured analysis methodology lets you evaluate how key tradeoffs affect voltage and timing margins, providing objective data for making design decisions.

THE MOST CERTIFIED SERDES SIMULATION MODELS

SiSoft drove development of the IBIS-AMI modeling standard and delivered the first reference models, test bench and commercial simulation tools. Working together with our semiconductor partners, SiSoft has developed and collaborated on more IBIS-AMI models and design kits than anyone. Contact your SiSoft representative for the latest information on available QCD Design Kits.

THE BROADEST CORRELATION

SiSoft presented the Industry's first IBIS-AMI performance and correlation results in mid 2008. Working with our semiconductor partners, **we've correlated more IBIS-AMI models to both reference simulations and hardware measurements than anyone**. More information on our correlation work can be found on SiSoft's eLearning web site, www.sisoft.com/elearning.

AUTOMATED STANDARDS COMPLIANCE

QCD Compliance Kits include automated Design Rule Checks for popular interface standards like PCI-Express 1/2/3, Ethernet 802.3xx and others. QCD analyzes your design for compliance with time - and frequency - domain masks, automatically flagging violations. Key standards-based design metrics are also computed and reported, with violations automatically flagged.

## BACKED BY SISOFT'S EXPERIENCE IN HIGH-SPEED SYSTEMS DESIGN

SiSoft's staff of recognized industry experts keeps SiSoft's products at the forefront of high-speed design by using them every day to perform state-of-the-art design and analysis. SiSoft provides a full range of model development, design analysis and methodology training services. SiSoft's consultants can analyze your high-speed design for you, or provide the tools and training you need to perform high-speed design analysis in-house.

CAD LAYOUT SYSTEM SUPPORT

Allegro®, Expedition PCB™, PowerPCB™, Board Station®, Pantheon®, Altium Designer, Zuken CR-5000
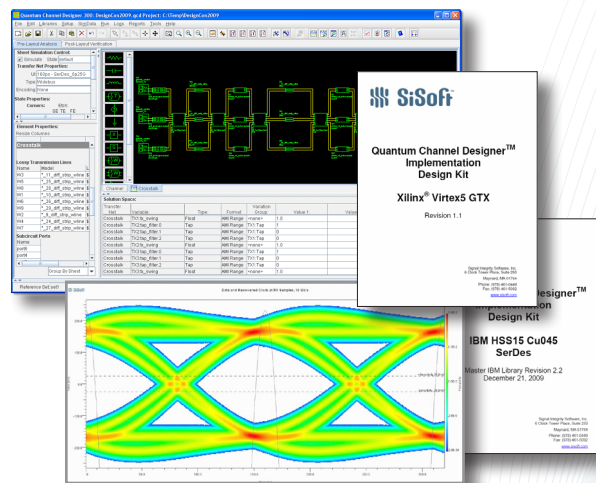
QCD Design Kits provide ready to run simulation setups
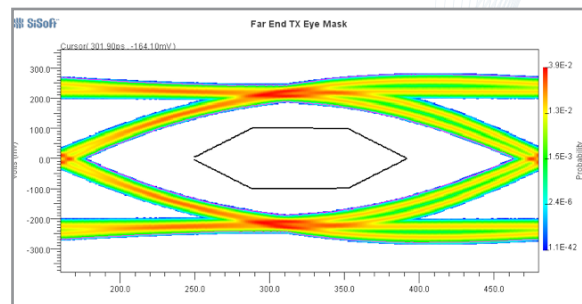
QCD Compliance Kits include Design Rule Checks for popular Interface Standards

To learn more about SiSoft's products, contact sales@sisoft. com or visit our website at www.sisoft.com.

⦚⦚ SiSoft™
We Are Signal Integrity

Signal Integrity Software, Inc.
6 Clock Tower Place, #250, Maynard, MA 01754
Phone: 978.461.0449   Fax: 978.461.5092