Essentials of 7 Series FPGAs

FPGA 2

7S-20000-14-ILT (v1.0H)

Course Specification

Course Description

This course introduces designers to the basic concepts of 7 Series FPGAs, specifically on how to efficiently utilize CLB architecture, Memory resources and DSP resources in their designs. Modules associated with the individual resources are immediately followed by a lab exercise.

The course starts with an overview of the 7 Series FPGA families and then, details the architectural features of the devices.

Level – FPGA 2

Course Duration – 5-8 hours (available online for 30 days)

Price – $700 or 7 Training Credits

Course Part Number – 7S-20000-14-ILT

Who Should Attend? – Digital designers who have a working knowledge of HDL (VHDL or Verilog) and who are new to Xilinx FPGAs

Prerequisites

- *Essentials of FPGA Design* (14.1v or earlier)
- Intermediate VHDL or Verilog knowledge

You should be able to describe the following as part of the prerequisites for this course as this material will not be reviewed.

- Describe the basic Xilinx software flow
- Describe the basic implementation options of the ISE® tools
- Describe global timing and I/O constraints

Software

- Xilinx ISE® Design Suite

Hardware

- None

* This course focuses on the 7 series architecture. Check with Hardent for the specifics of the in-class lab board or other customizations.

After completing this comprehensive training, you will have the necessary skills to:

- Describe the functionality of the 6-input LUT and the CLB construction of the 7 Series FPGAs
- Specify the CLB resources and the available slice configurations for the 7 Series FPGAs
- Define the block RAM, FIFO, and DSP resources available for the 7 Series FPGAs
- Properly design for the I/O block and SERDES resources in the 7 Series FPGAs

Course Outline

Day 1

- 7 Series FPGA Overview
- CLB Architecture
- Slice Flip-Flops
- Lab 1: CLB Resources
- Memory Resources
- Lab 2: Memory Resources
- DSP Resources
- Lab 3: DSP Resources

Lab Descriptions

- **Lab 1:** CLB Resources – Complete the code for a 32-bit counter design and use the RTL technologies schematic viewers and FPGA editor to examine the design after various steps in the implication process.
- **Lab 2:** Memory Resources – Complete the code for a read-first, true dual-port memory; use the schematic viewers and FPGA editor to analyze the design at various stages; modify the code to implement a write-first memory and finally, infer a true dual-port block RAM in both read-first and write-first modes.
- **Lab 3:** DSP Resources – Complete the code for a 24 by 17 bit multiply accumulate design; use the FPGA editor to view the design after different steps in the implementation process; create a wide pipeline multiplier, instantiate it in your design and analyze the resulting structure.

Register Today

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