Colibri T30

Preliminary Datasheet

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Revision History

Date	Doc. Rev.	Colibri T30 Version	Changes
14-Dec-2012	Rev. 1.0	V1.1B	Initial Release: Preliminary version

Contents

1. Introduction

1.1 Hardware

The Colibri T30 is a SODIMM sized computer module based on the NVIDIA© Tegra 3 embedded System-on-Chip (SoC). The Cortex A9 quad core CPU peaks at 1.4 GHz. The module delivers very high CPU and graphic performance with minimum power consumption. The Colibri T30 incorporates DVFS (Dynamic Voltage and Frequency Switching) and Thermal Throttling which enables the system to continuously adjust operating frequency and voltage in response to changes in workload and temperature to achieve the best performance with the lowest power consumption.

The integrated NVIDIA Graphics enables visually rich, smooth and fast user interfaces.

The module targets a wide range of applications, including: Digital Signage, Medical Devices, Navigation, Industrial Automation, HMIs, Avionics, Entertainment System, POS, Data Acquisition, Thin Clients, Robotics, Gaming and much more

It offers a wide range of interfaces from simple GPIOs, industry standard I2C and SPI buses through to high speed USB 2.0 interfaces and a high speed memory bus. The HDMI interface makes it very easy to connect large, full HD resolution displays.

Existing customers will benefit from an extremely easy migration path from the current Colibri PXAxxx or Colibri T20 module range to the Colibri T30 – all Colibri modules are electrically pin compatible. New customers will also appreciate the ability to select the Colibri module most suitable for their application to achieve the optimum price/performance balance without the need to support different carrier board designs.

1.2 Software

Initially, the Colibri T30 will be provided with an embedded Linux Image.
Additionally a Windows Embedded Compact Image is in the works and will be available soon.

Toradex works with partners in case you require another Operating System. For more information contact our support.

1.3 Main Features

1.3.1 CPU

- ✓ NVIDIA Tegra 3 4-PLUS-1 quad-core Cortex-A9 MPcore
- ✓ ARM Cortex-A9 ultra low power shadow processor
- ✓ All cores have 32KB Instruction and 32KB Data Level 1 caches
- ✓ 1MB shared Level 2 cache
- ✓ NEON Support
- ✓ 1.4 GHz Single Core mode
- ✓ 1.2 GHz Quad Core mode peak performance (Time/Temperature limited)
- ✓ 900MHz Quad Core mode constant performance (constant performance at max Temperature)

1.3.2 Memory

- ✓ 1GByte DDR3 (32 Bit)
- ✓ 2GByte NAND FLASH (8 Bit eMMC)

1.3.3 Interfaces

- ✓ LCD RGB (2048 x 1536)
- ✓ HDMI 1.4a 1080p60 (1920x1080) (3D Video Format support)
- ✓ Analog Video (1920x1200) (not currently supported in Linux)
- ✓ Touch Screen (4 wire)
- ✓ Audio I/O
- ✓ Camera Interface
- ✓ 3x I2C
- ✓ 5x SPI
- ✓ 5x UART
- ✓ 2x SDCard/MMC 4Bit
- ✓ Up to 110 GPIOs
- ✓ USB 2.0 high speed OTG (host/device)
- ✓ USB 2.0 high speed host
- ✓ 10/100 Mbit Ethernet
- ✓ One-Wire
- ✓ Keypad
- ✓ 4x PWM
- ✓ S/PDIF
- ✓ I2S

1.3.4 HD Video Decode

- ✓ H.264 (Baseline Profile ,Main Profile, High Profile) — 1080p@48, 1080p@30, 1080p60
- ✓ WMV9 VC-1 (Simple, Main and Advanced Profiles) — 1080p@30, 1080i@60
- ✓ MPEG-4 (Simple + B frames) — 1080p@30
- ✓ MPEG-2 (Main Profile) — 1080p@30, 1080i@60
- ✓ H.263 (Profile 0) — 1080p@30
- ✓ DiVX 4/5/6 (Home Theater Profile) — 1080p@30
- ✓ XviD — 1080p/30Mbps

- ✓ JPEG up to 120 MPixel per second

1.3.5 HD Video Encode

- ✓ H.264 (Baseline Profile) — 1080p/30Mbps
- ✓ MPEG-4 (Simple Profile) — 1080p@24
- ✓ H.263 (Profile 0) — 1080p@24
- ✓ JPEG up to 120 MPixel per second

1.3.6 Ultra-low Power NVIDIA GeForce GPU

- ✓ OpenGL® ES 2.0
- ✓ Dual Core (2 fragment shader pipe, vertex shader pipe)
- ✓ OpenGL ES Shader Performance 16 GFLOPS
- ✓ Programmable pixel shader
- ✓ Programmable vertex and lighting
- ✓ Anti-aliasing: 5x VCAA, 4xFSAA, or both
- ✓ 2K x 2K texture and 4K x 4K render resolutions supported
- ✓ Advanced 2D and vector engine

1.3.7 3D Vision (Support requires additional license and royalty fee)

- ✓ Automatic Stereo
- ✓ Built-in (native) pixel Interleaving support
- ✓ 3D Video and Photo Capture
- ✓ 3D Video and Photo Playback
- ✓ HDMI 1.4a Frame packing 1080p24

1.3.8 Digital Audio Decode

- ✓ AAC-LC, AAC, AAC+, eAAC+
- ✓ WMA7/8/9, WMA Lossless, WMA Pro LBR 10,
- ✓ MP3
- ✓ AC3
- ✓ MPEG2
- ✓ WAVE

1.3.9 Digital Audio Encode

- ✓ AAC-LC
- ✓ AMR-WB / AMR-NB

1.3.10 Timers

- ✓ 10 timers
- ✓ 1 Micro Second resolution
- ✓ Watchdog function

1.3.11 Supported Operating Systems

- ✓ Embedded Linux
- ✓ Windows Embedded Compact 7.0 planned
- ✓ Contact Toradex for Android
- ✓ Other operating systems are available through 3rd party companies

1.4 Reference Documents

1.4.1 Nvidia Tegra T30

You will find the details about T30 chip in the Datasheet and Technical Reference Manual provided by Nvidia. (Registration required)

https://developer.nvidia.com/tegra-3-technical-reference-manual

1.4.2 Ethernet Controller

Colibri T30 uses the Asix AX88772B Ethernet chip
http://www.asix.com.tw

1.4.3 Audio Codec

Colibri T30 uses the Freescale SGTL5000 Audio Codec.
http://www.freescale.com/

1.4.4 Touch Screen Controller / ADC

Colibri T30 uses the STMicroelectronics STMPE811 Touchscreen Controller.
http://www.st.com

1.4.5 Toradex Migration Guide

This document provides additional information about the pin usage and describes functional compatibility with the rest of the Colibri family. Please study this document in detail prior to starting your carrier board design.
http://www.toradex.com/Products/Colibri_Modules

1.4.6 Toradex Developer Center

You can find a lot of additional information in the Toradex Developer Center, which is updated with the latest product support information on a regular basis.
Please note that the Developer Center is common for all Toradex products. You should always check to ensure if information is valid or relevant for the Colibri T30.
http://www.developer.toradex.com

1.4.7 Iris Board Schematics

We provide the completed schematics plus the Altium project file for the Iris Carrier board and the Colibri Evaluation Board for free. This is a great help when designing your own Carrier Board.
http://developer.toradex.com/hardware-resources/arm-family/carrier-board-design

2. Architecture Overview

2.1 Block Diagram

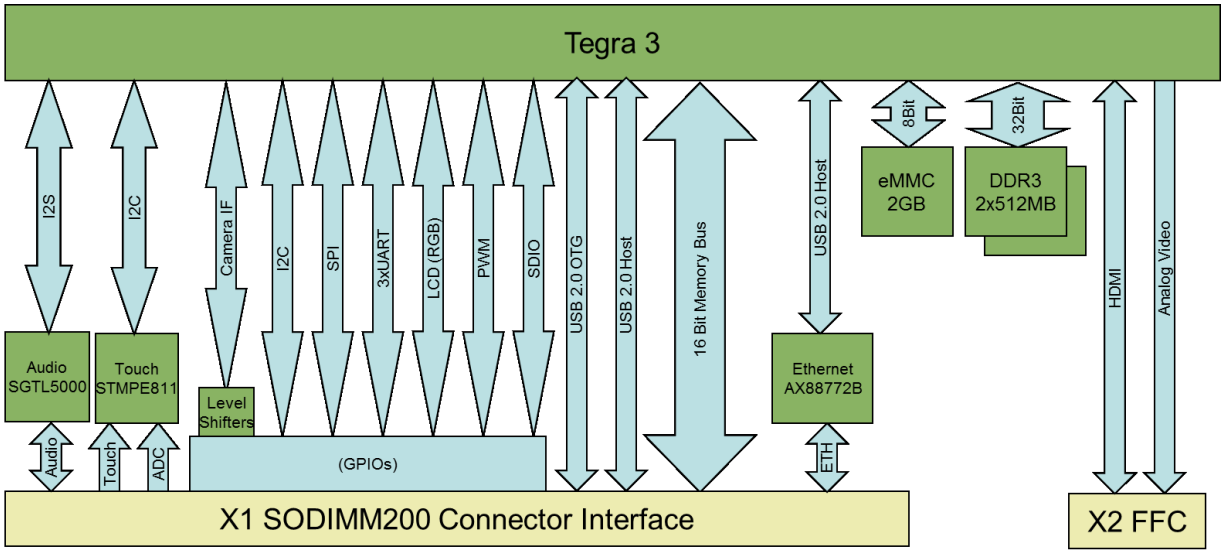


Figure 1 Colibri T30 Block Diagram

3. Colibri T30 Connectors

3.1 Physical Locations

The Colibri T30 is equipped with a 200 Pin SODIMM edge connector (X1) and an FCC connector (X2). The position of the connectors is shown in the figure below.

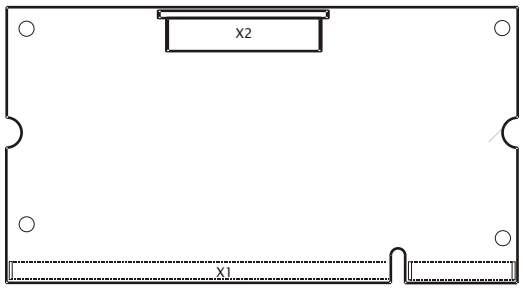


Figure 2 Location of the Colibri T30 connectors. (Bottom of the module)

3.2 Assignment

3.2.1 SODIMM 200

The following table describes the SODIMM 200 way connector pin out. It should be noted that some of the pins are multiplexed; this means there is more than one Tegra pin connected to one SODIMM or FFC pin. For example, SDMMC3_CMD and VI_D6 are both assigned to SODIMM pin 67. Care should be taken to ensure that multiplexed Tegra pins are tri-stated when they are not being used (e.g., if Tegra pin A and pin B are tied to SODIMM pin 1, then if you are driving Tegra pin A, then pin B should be tri-stated). Additional information can be found in chapter 4.1: Function Multiplexing.

- X1 Pin: Pin number on the SODIMM connector (X1).
- Compatible function: The default function which is compatible with all Colibri modules.
  IMPORTANT: There are some limitations. You can find more information about pin compatibility in the "**Colibri Migration Guide**".
- Tegra 3 Pin Name: The name of the pin of the Tegra chip.
- GPIO Name: The name of the GPIO function which is available on this pin.

Table 3-1 X1 Connector

X1 Pin	Compatible Function	Tegra 3 Pin Name	GPIO Name	X1 Pin	Compatible Function	Tegra 3 Pin Name	GPIO Name
1	MIC_IN			2	AD3		
3	MIC_GND			4	AD2		
5	LINEIN_L			6	AD1		
7	LINEIN_R			8	AD0		

X1 Pin	Compatible Function	Tegra 3 Pin Name	GPIO Name
9	VSS_AUDIO		
11	VSS_AUDIO		
13	HEADPHONE_GND		
15	HEADPHONE_L		
17	HEADPHONE_R		
19	STD_RXD	UART2_RXD	GPIO-C.03
21	STD_TXD	UART2_TXD	GPIO-C.02
23	FF_DTR	ULPI_DATA7	GPIO-O.00
25	FF_CTS	ULPI_DATA2	GPIO-O.03
27	FF_RTS/SSPSYSCLK	ULPI_DATA3	GPIO-O.04
29	FF_DSR	ULPI_DATA6	GPIO-O.07
31	FF_DCD	ULPI_DATA5	GPIO-O.06
33	FF_RXD	ULPI_DATA1	GPIO-O.02
35	FF_TXD	ULPI_DATA0	GPIO-O.01
37	FF_RI	ULPI_DATA4	GPIO-O.05
39	GND		
41	GND		
43	MMC_CD(GPIO)/ WAKE0	GMI_WP_N	GPIO-C.07
45	PRDY(GPIO)/WAKE 1	GPIO_PV1	GPIO-V.01
47	MMC_CLK	CAM_MCLK	GPIO-CC.00
49	MMC_DAT1	CAM_I2C_SCL	GPIO-BB.01
51	MMC_DAT2	CAM_I2C_SDA	GPIO-BB.02
53	MMC_DAT3	GPIO_PBB3	GPIO-BB.03
55	PS2_SDA1(GPIO)	SDMMC3_DAT1	GPIO-B.06
57	LDD16	LCD_D16	GPIO-M.00
59	PWM_A/CIF_DD7	SDMMC3_DAT3	GPIO-B.04
61	LDD17	LCD_D17	GPIO-M.01
63	PS2_SCL1(GPIO)	SDMMC3_DAT0	GPIO-B.07
65	PS2_SDA2(GPIO)/ CIF_DD9	PEX_L1_CLKREQ_N	GPIO-DD.06
67	PWM_D/CIF_DD6	SDMMC3_CMD	GPIO-A.07
69	PS2_SCL2(GPIO)/ CIF_DD10	PEX_L1_RST_N	GPIO-DD.05
71	BL_ON(GPIO)/ CIF_DD0	GPIO_PV2	GPIO-V.02
73	CAN_INT(GPIO)	KB_ROW8	GPIO-S.00
75	PRST(GPIO)/ CIF_MCLK	CLK2_OUT	GPIO-W.05

X1 Pin	Compatible Function	Tegra 3 Pin Name	GPIO Name
10	AVDD_AUDIO		
12	AVDD_AUDIO		
14	TSPX		
16	TSMX		
18	TSPY		
20	TSMY		
22	nVDD_FAULT (SENSE)	PEX_L2_PRSNT_N	GPIO-DD.07
24	nBATT_FAULT (SENSE)	PEX_L2_RST_N	GPIO-CC.06
26	nRESET_EXT		
28	PWM_B	SDMMC3_DAT2	GPIO-B.05
30	PWM_C	SDMMC3_CLK	GPIO-A.06
32	BT_CTS	GMI_A18	GPIO-B.01
34	BT_RTS	GMI_A19	GPIO-K.07
36	BT_RXD	GMI_A17	GPIO-B.00
38	BT_TXD	GMI_A16	GPIO-J.07
40	VCC_BATT		
42	3V3		
44	L_BIAS	LCD_DE	GPIO-J.01
46	LDD7	LCD_D7	GPIO-E.07
48	LDD9	LCD_D9	GPIO-F.01
50	LDD11	LCD_D11	GPIO-F.03
52	LDD12	LCD_D12	GPIO-F.04
54	LDD13	LCD_D13	GPIO-F.05
56	L_PCLK_WR	LCD_PCLK	GPIO-B.03
58	LDD3	LCD_D3	GPIO-E.03
60	LDD2	LCD_D2	GPIO-E.02
62	LDD8	LCD_D8	GPIO-F.00
64	LDD15	LCD_D15	GPIO-F.07
66	LDD14	LCD_D14	GPIO-F.06
68	L_LCLK_A0	LCD_HSYNC	GPIO-J.03
70	LDD1	LCD_D1	GPIO-E.01
72	LDD5	LCD_D5	GPIO-E.05
74	LDD10	LCD_D10	GPIO-F.02
76	LDD0	LCD_D0	GPIO-E.00

X1 Pin	Compatible Function	Tegra 3 Pin Name	GPIO Name
77	PBVD2(GPIO)/ CIF_DD11	GPIO_PCC2	GPIO-CC.02
79	PBVD1(GPIO)/ CIF_DD4	SDMMC1_DAT2	GPIO-Y.05
81	PCD(GPIO)/ CIF_FV	LCD_PWR1	GPIO-C.01
83	GND		
85	nPPEN(GPIO)/ CIF_DD8	GPIO_PV3	GPIO-V.03
87	nRESET_OUT	GMI_RST_N	GPIO-I.04
89	nWE	GMI_WR_N	GPIO-I.00
91	nOE	GMI_OE_N	GPIO-I.01
93	RDnWR	LCD_CS1_N	GPIO-W.00
95	RDY	GMI_WAIT	GPIO-I.07
97	nPOE/CIF_DD5	SDMMC1_DAT3	GPIO-Y.04
99	nPWE	LCD_WR_N	GPIO-Z.03
101	nPIOW/CIF_DD2	SDMMC1_DAT0	GPIO-Y.07
103	nPIOR/CIF_DD3	SDMMC1_DAT1	GPIO-Y.06
105	nEXT_CS0(CAN)	GMI_CS4_N	GPIO-K.02
107	nEXT_CS1	GMI_CS2_N	GPIO-K.03
109	GND		
111		UART2_RTS_N	GPIO-J.06
113		UART2_CTS_N	GPIO-J.05
115		UART3_TXD	GPIO-W.06
117		UART3_RXD	GPIO-W.07
119		UART3_RTS_N	GPIO-C.00
121		UART3_CTS_N	GPIO-A.01
123		GPIO_PU0	GPIO-U.00
125		GPIO_PU1	GPIO-U.01
127	EXT_IO2(GPIO)	GEN2_I2C_SDA	GPIO-T.06
129	USBH_PEN	SPI2_CS1_N	GPIO-W.02
131	USBH_OC	SPI2_CS2_N	GPIO-W.03
133	EXT_IO1(GPIO)	GEN2_I2C_SCL	GPIO-T.05
135	EXT_IO0(GPIO)/ USB_ID(GPIO)	ACC1_DETECT	
137	USBC_DET(GPIO)	USB1_VBUS	
139	USBH_P	USB3_DP	
141	USBH_N	USB3_DN	
143	USBC_P	USB1_DP	
145	USBC_N	USB1_DN	
147	GND		

X1 Pin	Compatible Function	Tegra 3 Pin Name	GPIO Name
78	LDD4	LCD_D4	GPIO-E.04
80	LDD6	LCD_D6	GPIO-E.06
82	L_FCLK_RD	LCD_VSYNC	GPIO-J.04
84	3V3		
86	SSPFRM	ULPI_STP	GPIO-Y.03
88	SPSCLK	ULPI_NXT	GPIO-Y.02
90	SSPRXD	ULPI_DIR	GPIO-Y.01
92	SSPTXD	ULPI_CLK	GPIO-Y.00
94	nPCE1/CIF_LV	PEX_L2_CLKREQ_N	GPIO-CC.07
96	nPCE2/CIF_PCLK	SDMMC1_CLK	GPIO-Z.00
98	nPREG/CIF_DD1	SDMMC1_CMD	GPIO-Z.01
100	nPXCVREN	SPI1_SCK	GPIO-X.05
102	nPWAIT	SPI1_CS0_N	GPIO-X.06
104	nIOIS16	SPI1_MISO	GPIO-X.07
106	nEXT_CS2	GMI_CS3_N	GPIO-K.04
108	3V3		
110		GPIO_PU2	GPIO-U.02
112		GPIO_PU3	GPIO-U.03
114		GPIO_PU4	GPIO-U.04
116		GPIO_PU5	GPIO-U.05
118		GPIO_PU6	GPIO-U.06
120		DAP4_FS	GPIO-P.04
122		DAP4_DIN	GPIO-P.05
124		DAP4_DOUT	GPIO-P.06
126		GMI_CS0_N	GPIO-J.00
128		GMI_CS1_N	GPIO-J.02
130		GMI_CS6_N	GPIO-I.03
132		GMI_CS7_N	GPIO-I.06
134		SPI1_MOSI	GPIO-X.04
136	LDD18	SPI2_CS0_N	GPIO-X.03
138	LDD19	SPI2_SCK	GPIO-X.02
140	LDD20	SPI2_MISO	GPIO-X.01
142	LDD21	SPI2_MOSI	GPIO-X.00
144	LDD22	DAP2_DOUT	GPIO-A.05
146	LDD23	DAP2_DIN	GPIO-A.04
148	3V3		

X1 Pin	Compatible Function	Tegra 3 Pin Name	GPIO Name
149		GMI_AD0	GPIO-G.00
151		GMI_AD1	GPIO-G.01
153		GMI_AD2	GPIO-G.02
155		GMI_AD3	GPIO-G.03
157		GMI_AD4	GPIO-G.04
159		GMI_AD5	GPIO-G.05
161		GMI_AD6	GPIO-G.06
163		GMI_AD7	GPIO-G.07
165		GMI_AD8	GPIO-H.00
167		GMI_AD9	GPIO-H.01
169		GMI_AD10	GPIO-H.02
171		GMI_AD11	GPIO-H.03
173		GMI_AD12	GPIO-H.04
175		GMI_AD13	GPIO-H.05
177		GMI_AD14	GPIO-H.06
179		GMI_AD15	GPIO-H.07
181	GND		
183	LAN_LINK_AKT		
185	LAN_SEED100		
187	LAN_TXO-		
189	LAN_TXO+		
191	LAN_AGND		
193	LAN_RXI-		
195	LAN_RXI+		
197	GND		
199	GND		

X1 Pin	Compatible Function	Tegra 3 Pin Name	GPIO Name
150		GMI_ADV_N	GPIO-K.00
152		GMI_CLK	GPIO-K.01
154		LCD_PWR0	GPIO-B.02
156		LCD_SDIN	GPIO-Z.02
158		LCD_SDOUT	GPIO-N.05
160		LCD_CS0_N	GPIO-N.04
162		LCD_DC0	GPIO-N.06
164		LCD_SCK	GPIO-Z.04
166		GPIO_PBB4	GPIO-BB.04
168		GPIO_PBB5	GPIO-BB.05
170		GPIO_PBB6	GPIO-BB.06
172		GPIO_PBB7	GPIO-BB.07
174		DAP1_FS	GPIO-N.00
176		DAP1_DIN	GPIO-N.01
178		DAP1_DOUT	GPIO-N.02
180		DAP1_SCLK	GPIO-N.03
182	3V3		
184		DAP2_SCLK	GPIO-A.03
186		DAP2_FS	GPIO-A.02
188		DAP4_SCLK	GPIO-P.07
190	MMC_CMD	GPIO_PCC1	GPIO-CC.01
192	MMC_DAT0	GPIO_PBB0	GPIO-BB.00
194	I2C_SDA	GEN1_I2C_SDA	GPIO-C.05
196	I2C_SCL	GEN1_I2C_SCL	GPIO-C.04
198	3V3		
200	3V3		

3.2.2 HDMI

This connector is compatible with the Colibri T20 but not backward compatible with the Colibri PXAxxx family. Its primary purpose is to provide the signals for the HDMI/DVI and analog (VGA) display interface. The only pin on this connecter which provides a GPIO function is pin 14
(GPIO_N7).

Table 3-2 X2 Connector

Pin	Name	Description	Direction
1	GND (Shield)		
2	TMDS_CLK_P	Transmit Clock Positive	O
3	TMDS_CLK_N	Transmit Clock Negative	O
4	GND		

Pin	Name	Description	Direction
5	TMDS_DATA0_P	Data Lane 0 Positive	O
	TMDS_DATA0_N	Data Lane 0 Negative	O
7	GND		
8	TMDS_DATA1_P	Data Lane 1 Positive	O
9	TMDS_DATA1_N	Data Lane 1 Negative	O
10	GND		
11	TMDS_DATA2_P	Data Lane 2 Positive	O
12	TMDS_DATA2_N	Data Lane 2 Negative	O
13	3V3_DDC_OUT		O
14	HOTPLUG_DETECT	Hot Plug Detection, 5V Tolerant, 100K Ohm pull down on Colibri. 1K Ohm Serie resistor on base board recommended	I
15	DDC_SCL	DDC Serial Clock used for HDMI and the VGA interface. Open Collector Output 5V tolerant. To communicate with an HDMI/VGA display you need to pull up this line to 5V.	O
16	DDC_SDA	Serial Data. See DDC_SCL description	I/O
17	GND		
18	VGA_RED	Red signal for Analog RGB and Component TV out connections. For TV S-Video Output, this carries the color (chrominance) information.*	O
19	GND		
20	VGA_GREEN	Green signal for Analog RGB and Component TV out connections. For TV S-Video Output, this carries the intensity (Luminance) information. Also used for Composite TV Output when this is the only TV Output interface.*	O
21	GND		
22	VGA_BLUE	Blue signal for Analog RGB and Composite TV out connections. Used for Composite TV out when VGA_RED and VGA_GREEN are used for S-Video out.*	O
23	VGA_VSYNC	Vertical Sync for Analog RGB (VGA) Interface. It is recommended to level shift this signal before going to the monitor. (Typically 5V)	O
24	VGA_HSYNC	Horizontal Sync for Analog RGB (VGA) Interface. It is recommended to level shift this signal before going to the monitor. (Typically 5V)	O

*Please contact Toradex if you plan to use Composite or S-Video Interface.

4. I/O Pins

4.1 Function Multiplexing

Most of the NVIDIA Tegra Processors I/O pins have up to four special functions. They can be used as "normal" GPIOs (General Purpose I/O, sometimes also referred to as Digital I/O).
For example, the Tegra Pin on connector X1, pin 21, has the primary function UART2-TXD, but can also provide the following alternative functions: SPDIF1.C-IN, UART1.C-RTS_N or SPI4.B-SCK.

The default setting for this pin is the primary function UART2-TXD. It is strongly recommended whenever possible to use a pin for a function which is compatible with all Colibri modules. This guarantees the best compatibility with the standard software and with the other modules in the Colibri family.

All of the pins in the Tegra family are organized into groups. For the Tegra T20, it was only possible to change the alternative function by groups. This limitation does not exist for Tegra T30. The alternative functions can now be changed individually by pin. The following pad control register still exist only per group and can therefore not be changed per pin:

- HSM High Speed Mode (Enable/Disable)
- SCHMT Schmitt Trigger (Enable/Disable)
- LPMD Low Power Mode
- DRVDN/UP Drive Down / Up
- SLWR/SLWF Slew Falling Rising

Most of the alternative functions are available on more than one pin. Care should be taken to ensure that two pins are not configured with the same function. This could lead to system instability and undefined behavior.

In some cases, the available alternative functions of certain pins on the Tegra device were constrained; to allow maximum flexibility; some of these pins are paired and share the same SODIMM pin. As previously mentioned, ensure that the unused pin in the pair is tri-stated to avoid undesired behavior and/or hardware damage.
The following X1 connector pins are connected to more than one Tegra:

Table 4-1 Colibri Multiplexed Pins

X1 Pin #	Tegra Pin 1	Tegra Pin 2	Remarks
44	LCD_DE	LCD_M1	
47	CAM_MCLK	KB_ROW10	
49	CAM_I2C_SCL	KB_ROW13	
51	CAM_I2C_SDA	KB_ROW14	
53	GPIO_PBB3	KB_ROW15	

X1 Pin #	Tegra Pin 1	Tegra Pin 2	Remarks
59	SDMMC3_DAT3	VI_D7	Due to the unidirectional level shifter, VI_D7 can only be used as input, use SDMMC3_DAT3 if general purpose output functionality is needed. See also Figure 3.
65	PEX_L1_CLKREQ_N	VI_D9	Due to the unidirectional level shifter, VI_D9 can only be used as input, use PEX_L1_CLKREQ_N if general purpose output functionality is needed. (Similar to Figure 3)
67	SDMMC3_CMD	VI_D6	Due to the unidirectional level shifter, VI_D6 can only be used as input, use SDMMC3_CMD if general purpose output functionality is needed. (Similar to Figure 3)
69	PEX_L1_RST_N	VI_D10	Due to the unidirectional level shifter, VI_D10 can only be used as input, use PEX_L1_RST_N if general purpose output functionality is needed. (Similar to Figure 3)
71	GPIO_PV2	VI_D0	Due to the unidirectional level shifter, VI_D0 can only be used as input, use GPIO_PV2 if general purpose output functionality is needed. (Similar to Figure 3)
77	GPIO_PCC2	VI_D11	Due to the unidirectional level shifter, VI_D11 can only be used as input, use GPIO_PCC2 if general purpose output functionality is needed. (Similar to Figure 3)
79	SDMMC1_DAT2	VI_D4	Due to the unidirectional level shifter, VI_D4 can only be used as input, use SDMMC1_DAT2 if general purpose output functionality is needed. (Similar to Figure 3)
81	LCD_PWR1	VI_VSYNC	Due to the unidirectional level shifter, VI_VSYNC can only be used as input, use LCD_PWR1 if general purpose output functionality is needed. (Similar to Figure 3)
85	GPIO_PV3	VI_D8	Due to the unidirectional level shifter, VI_D8 can only be used as input, use GPIO_PV3 if general purpose output functionality is needed. (Similar to Figure 3)
86	ULPI_STP	SDMMC3_DAT6	
92	ULPI_CLK	SDMMC3_DAT7	
93	LCD_CS1_N	GMI_WR_N	GMI_WR_N is connected via a 3-State buffer with LCD_CS1_N. To tristate the buffer set SDMMC3_DAT5 (GPIO-D.00) to high. (default state). For more information see the Figure 4.
94	PEX_L2_CLKREQ_N	VI_HSYNC	Due to the unidirectional level shifter, VI_HSYNC can only be used as input, use PEX_L2_CLKREQ_N if general purpose output functionality is needed. (Similar to Figure 3)
95	GMI_WAIT	GMI_IORDY	
96	SDMMC1_CLK	VI_PCLK	Due to the unidirectional level shifter, VI_PCLK can only be used as input, use SDMMC1_CLK if general purpose output functionality is needed. (Similar to Figure 3)
97	SDMMC1_DAT3	VI_D5	Due to the unidirectional level shifter, VI_D5 can only be used as input, use SDMMC1_DAT3 if general purpose output functionality is needed. (Similar to Figure 3)
98	SDMMC1_CMD	VI_D1	Due to the unidirectional level shifter, VI_D1 can only be used as input, use SDMMC1_CMD if general purpose output functionality is needed. (Similar to Figure 3)

X1 Pin #	Tegra Pin 1	Tegra Pin 2	Remarks
99	LCD_WR_N	GMI_WR_N	GMI_WR_N is connected via a 3-State buffer with LCD_WR_N. To tristate the buffer set SDMMC3_DAT4 (GPIO-D.01) to high. (default state). For more information see the Figure 4.
101	SDMMC1_DAT0	VI_D2	Due to the unidirectional level shifter, VI_D2 can only be used as input, use SDMMC1_DAT0 if general purpose output functionality is needed. (Similar to Figure 3)
103	SDMMC1_DAT1	VI_D3	Due to the unidirectional level shifter, VI_D3 can only be used as input, use SDMMC1_DAT1 if general purpose output functionality is needed. (Similar to Figure 3)
135	ACC1_DETECT	SPDIF_IN	
136	SPI2_CS0_N	LCD_D18	Pulled up with 45K Ohm on the Colibri
137	USB1_VBUS	SPDIF_OUT	
138	SPI2_SCK	LCD_D19	Pulled up with 45K Ohm on the Colibri
140	SPI2_MISO	LCD_D20	
142	SPI2_MOSI	LCD_D21	
144	DAP2_DOUT	LCD_D22	
146	DAP2_DIN	LCD_D23	
152	GMI_CLK	OWR	
190	GPIO_PCC1	KB_ROW11	
192	GPIO_PBB0	KB_ROW12	

In the table in chapter 4.4 you will find a list of all pins which have alternative functions. There you can see which alternative function is available for each individual pin.

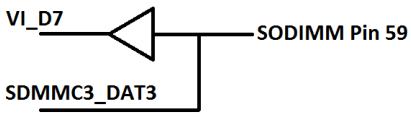
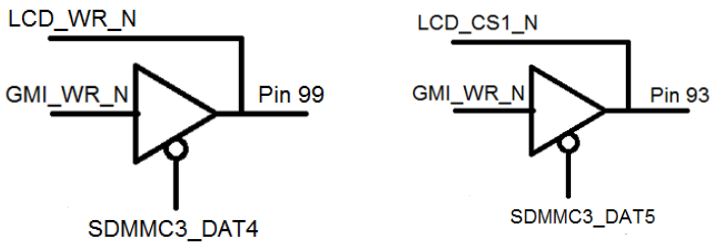


Figure 3



Buffer Control	Buffer Output
'0'	GMI_WR_N
'1'	HI_Z

Figure 4

4.2 Pin Control

The Tegra T30 pins that are connected to the X1 module connector are available in three different pad types. The following table describes the differences between the types:

Abbr.	Pad type	Input buffer	Output buffer	Nominal pull strength	Slew rate control	Drive strength control
ST	Standard	Schmitt / CMOS	Push- Pull	50kΩ or 100kΩ	2-bits, up & down	5-bits, up & down LPMD
DD	Dual driver	Schmitt / CMOS	Push-Pull / Open-Drain	50kΩ	2-bits, up & down	5-bits, up & down LPMD
CZ	Controlled output impedance	Schmitt / CMOS	Push- Pull	15kΩ	2-bits, up & down	7-bits, up & down
OD	Open drain	Schmitt / CMOS	Open-Drain	100kΩ down only	2-bits, down only	5-bits, down only LPMD
LV	Low voltage only camera interface	CMOS (level Shifter)	-	-	-	-

For each GPIO pin, the following controls can be changed individually if the function is available for this pad type:

- Output Enable Control: Normal I/O or tri-state
- Pull-up/down Control: Normal, pull up or pull
- Alternative Function Selection: Up to 4 special functions are available per pin.

If the following functions are available for this pad type, they can only be set for a whole pad group:

- High Speed Mode (Enable/Disable)
- Schmitt Trigger (Enable/Disable)
- Low Power Mode (LPMD)
- Drive strength control down / up
- Slew rate control falling / rising

4.3 Pin Reset Status

After a reset the pins can be in different modes. Most of them are tri-stated, pulled up or pulled low. A few are driven low or high. Please check the table in chapter 4.4 for a list of reset states for each of the pins. As soon as the bootloader is running, it is possible to reconfigure the pins and their states.

4.4 List Functions

Here you can find a list of all the Tegra pins which are available on the SODIMM connector X1. It shows what alternative functions are available for each pin. You will also find the Tegra GPIO name and the state of the pin immediately after reset (power on or software reset).

Reset Status Description

z: Tristate
pd: Pull Down
pu: Pull Up
pd+pu: Pulled Up and Pulled Down (due multiplexed pins)
0: Drive Low
1: Drive High

Function Short Forms

UART: Serial Ports (Universal Asynchronous Receiver/Transmitter)
VI: Video Interface (Camera Interface)
SPDIF: S/PDIF (Sony-Philips Digital Interface I/O)
SDIO: Secure Card I/O (SD, MMC, CE-ATA, eMMC)
HSMM: High Speed (SD, MMC, CE-ATA, eMMC)
SPI: Serial Peripheral Interface Bus
GMI: General Memory Interface
LCD: The parallel display interface
TWC: Three Wire Interface
OWR: One Wire Interface
DAP: Digital Audio Port (I2S and AC97)
PMFM: Pulse Width Modulation

X1 Pin	Tegra Pin Name	Primary Function	Alt 1	Alt 2	Alt 3	GPIO	Reset state	Pad Type	Pull Res. [KOhm]
19	UART2_RXD	UART2-RXD	SPDIF1.C-OUT	UART1.C-CTS_N	SPI4.B-MOSI	GPIO-C.03	pu	ST	100
21	UART2_TXD	UART2-TXD	SPDIF1.C-IN	UART1.C-RTS_N	SPI4.B-SCK	GPIO-C.02	pu	ST	100
22	PEX_L2_PRSNT_N	PEX2-PRSNT_N	HDA.D-SDI			GPIO-DD.07	z	ST	100
23	ULPI_DATA7	SPI2.A-CS1_N		UART1.A-DTR_N	ULPI-DATA7	GPIO-O.00	pu	ST	100
24	PEX_L2_RST_N	PEX2-RST_N	HDA.D-SDO			GPIO-CC.06	z	ST	100
25	ULPI_DATA2	SPI3.E-SCK		UART1.A-CTS_N	ULPI-DATA2	GPIO-O.03	pu	ST	100
27	ULPI_DATA3	SPI3.E-CS1_N		UART1.A-RTS_N	ULPI-DATA3	GPIO-O.04	pu	ST	100
28	SDMMC3_DAT2		PWFM-PWM1	SDMMC3-DAT2		GPIO-B.05	pu	CZ	15
29	ULPI_DATA6	SPI2.A-SCK		UART1.A-DSR_N	ULPI-DATA6	GPIO-O.07	pu	ST	100
30	SDMMC3_CLK	UART1.E-TXD	PWFM-PWM2	SDMMC3-SCLK		GPIO-A.06	pu	CZ	15
31	ULPI_DATA5	SPI2.A-MISO		UART1.A-DCD_N	ULPI-DATA5	GPIO-O.06	pu	ST	100
32	GMI_A18	UART4.B-CTS_N	SPI4.C-MISO	GMI-AD18	DTV-DATA	GPIO-B.01	z	ST	100
33	ULPI_DATA1	SPI3.E-MISO		UART1.A-RXD	ULPI-DATA1	GPIO-O.02	pu	ST	100
34	GMI_A19	UART4.B-RTS_N	SPI4.C-CS1_N	GMI-AD19		GPIO-K.07	z	ST	100
35	ULPI_DATA0	SPI3.E-MOSI		UART1.A-TXD	ULPI-DATA0	GPIO-O.01	pu	ST	100
36	GMI_A17	UART4.B-RXD	SPI4.C-MOSI	GMI-AD17	DTV-VALID	GPIO-B.00	z	ST	100
37	ULPI_DATA4	SPI2.A-MOSI		UART1.A-RI_N	ULPI-DATA4	GPIO-O.05	pu	ST	100
38	GMI_A16	UART4.B-TXD	SPI4.C-SCK	GMI-AD16	GMI-INT2	GPIO-J.07	z	ST	100
43	GMI_WP_N		NAND-CE5_N	GMI-WP_N	GMI-INT1	GPIO-C.07	pu	ST	100
44	LCD_DE	LCD0.A-DE	LCD1.A-DE			GPIO-J.01	pd	ST	100
44	LCD_M1	LCD0-M1	LCD1-M1			GPIO-W.01	pd	ST	100
45	GPIO_PV1					GPIO-V.01	z	ST	100
46	LCD_D7	LCD0-D7	LCD1-D7			GPIO-E.07	pd	ST	100
47	CAM_MCLK			CLK-VI_MCLK	SDMMC4.B-SCLK	GPIO-CC.00	pu	ST	50
47	KB_ROW10	KBC-ROW10	NAND_D10	SDMMC2.A-SCLK		GPIO-S.02	pd	ST	50
48	LCD_D9	LCD0-D9	LCD1-D9			GPIO-F.01	pd	ST	100

X1 Pin	Tegra Pin Name	Primary Function	Alt 1	Alt 2	Alt 3	GPIO	Reset state	Pad Type	Pull Res. [KOhm]
49	CAM_I2C_SCL		I2C3.A-CLK		SDMMC4.B-DAT1	GPIO-BB.01	z	DD	50
49	KB_ROW13	KBC-ROW13	NAND_D13	SDMMC2.A-DAT1		GPIO-S.05	pd	ST	50
50	LCD_D11	LCD0-D11	LCD1-D11			GPIO-F.03	pd	ST	100
51	CAM_I2C_SDA		I2C3.A-DAT		SDMMC4.B-DAT2	GPIO-BB.02	z	DD	50
51	KB_ROW14	KBC-ROW14	NAND_D14	SDMMC2.A-DAT2		GPIO-S.06	pd	ST	50
52	LCD_D12	LCD0-D12	LCD1-D12			GPIO-F.04	pd	ST	100
53	GPIO_PBB3	VI.A-VGP3	LCD0.C-DE	LCD1.C-DE	SDMMC4.B-DAT3	GPIO-BB.03	z	ST	50
53	KB_ROW15	KBC-ROW15	NAND_D15	SDMMC2.A-DAT3		GPIO-S.07	pd	ST	50
54	LCD_D13	LCD0-D13	LCD1-D13			GPIO-F.05	pd	ST	100
55	SDMMC3_DAT1			SDMMC3-DAT1		GPIO-B.06	pu	CZ	15
56	LCD_PCLK	LCD0.A-PCLK	LCD1.A-PCLK			GPIO-B.03	pd	ST	100
57	LCD_D16	LCD0-D16	LCD1-D16			GPIO-M.00	pd	ST	100
58	LCD_D3	LCD0-D3	LCD1-D3			GPIO-E.03	pd	ST	100
59	SDMMC3_DAT3		PWFM-PWM0	SDMMC3-DAT3		GPIO-B.04	pu	CZ	15
59	VI_D7		SDMMC2.B-DAT5	VI-D7		GPIO-L.05	pd	LV	15
60	LCD_D2	LCD0-D2	LCD1-D2			GPIO-E.02	pd	ST	100
61	LCD_D17	LCD0-D17	LCD1-D17			GPIO-M.01	pd	ST	100
62	LCD_D8	LCD0-D8	LCD1-D8			GPIO-F.00	pd	ST	100
63	SDMMC3_DAT0			SDMMC3-DAT0		GPIO-B.07	pu	CZ	15
64	LCD_D15	LCD0-D15	LCD1-D15			GPIO-F.07	pd	ST	100
65	PEX_L1_CLKREQ_N	PEXCLK1-CLKREQ_N	HDA.D-BCLK			GPIO-DD.06	z	ST	100
65	VI_D9		SDMMC2.B-DAT7	VI-D9		GPIO-L.07	pd	LV	15
66	LCD_D14	LCD0-D14	LCD1-D14			GPIO-F.06	pd	ST	100
67	SDMMC3_CMD	UART1.E-RXD	PWFM-PWM3	SDMMC3-CMD		GPIO-A.07	pu	CZ	15
67	VI_D6		SDMMC2.B-DAT4	VI-D6		GPIO-L.04	pd	LV	15
68	LCD_HSYNC	LCD0.A-HSYNC	LCD1.A-HSYNC			GPIO-J.03	pu	ST	100
69	PEX_L1_RST_N	PEX1-RST_N	HDA.D-RESET			GPIO-DD.05	z	ST	100
69	VI_D10			VI-D10		GPIO-T.02	pd	LV	15
70	LCD_D1	LCD0-D1	LCD1-D1			GPIO-E.01	pd	ST	100
71	GPIO_PV2	OWR-PCTLZ				GPIO-V.02	z	ST	100
71	VI_D0			VI-D0		GPIO-T.04	pd	LV	15
72	LCD_D5	LCD0-D5	LCD1-D5			GPIO-E.05	pd	ST	100
73	KB_ROW8	KBC-ROW8	NAND_D8	SDMMC2.A-DAT6		GPIO-S.00	pd	ST	50
74	LCD_D10	LCD0-D10	LCD1-D10			GPIO-F.02	pd	ST	100
75	CLK2_OUT	CLK-EXTCLK2				GPIO-W.05	pd	ST	100
76	LCD_D0	LCD0-D0	LCD1-D0			GPIO-E.00	pd	ST	100
77	GPIO_PCC2	I2S4.A-SCLK			SDMMC4.B-RST_N	GPIO-CC.02	pu	ST	50
77	VI_D11			VI-D11		GPIO-T.03	pd	LV	15
78	LCD_D4	LCD0-D4	LCD1-D4			GPIO-E.04	pd	ST	100
79	SDMMC1_DAT2	SDMMC1-DAT2		UART5.A-RXD		GPIO-Y.05	pu	CZ	15
79	VI_D4		SDMMC2.B-DAT2	VI-D4		GPIO-L.02	pd	LV	15
80	LCD_D6	LCD0-D6	LCD1-D6			GPIO-E.06	pd	ST	100
81	LCD_PWR1	LCD0-PW1	LCD1-PW1			GPIO-C.01	pd	ST	100
81	VI_VSYNC			VI-VSYNC		GPIO-D.06	pd	LV	15
82	LCD_VSYNC	LCD0.A-VSYNC	LCD1.A-VSYNC			GPIO-J.04	pu	ST	100
85	GPIO_PV3					GPIO-V.03	z	ST	100
85	VI_D8		SDMMC2.B-DAT6	VI-D8		GPIO-L.06	pd	LV	15
86	ULPI_STP	SPI1.A-CS0_N		UART4.A-RTS_N	ULPI-STP	GPIO-Y.03	z	ST	100
86	SDMMC3_DAT6	SPDIF1.B-IN		SDMMC3-DAT6		GPIO-D.03	pu	CZ	15
87	GMI_RST_N	NAND-BSY3	NAND-CLE	GMI-RST_N		GPIO-I.04	pu	ST	100[3]
88	ULPI_NXT	SPI1.A-SCK		UART4.A-CTS_N	ULPI-NXT	GPIO-Y.02	z	ST	100
89	GMI_WR_N		NAND-WE_N	GMI-WR_N		GPIO-I.00	1[4]	ST	100
90	ULPI_DIR	SPI1.A-MISO		UART4.A-RXD	ULPI-DIR	GPIO-Y.01	z	ST	100
91	GMI_OE_N		NAND-RE_N	GMI-OE_N		GPIO-I.01	1[4]	ST	100[1]
92	ULPI_CLK	SPI1.A-MOSI		UART4.A-TXD	ULPI-CLOCK	GPIO-Y.00	z	ST	100
92	SDMMC3_DAT7	SPDIF1.B-OUT		SDMMC3-DAT7		GPIO-D.04	pu	CZ	15
93	LCD_CS1_N	LCD0-M0	LCD1-M0	SPI5.B-CS3_N		GPIO-W.00	pu	ST	100
93	GMI_WR_N - Gated								
94	PEX_L2_CLKREQ_N	PEXCLK2-CLKREQ_N	HDA.D-SYNC			GPIO-CC.07	z	ST	100
94	VI_HSYNC			VI-HSYNC		GPIO-D.07	pd	LV	15
95	GMI_WAIT		NAND-BSY0	GMI-WAIT		GPIO-I.07	pu	ST	100
95	GMI_IORDY		NAND-CE3_N	GMI-IORDY		GPIO-I.05	pu	ST	100
96	SDMMC1_CLK	SDMMC1-SCLK				GPIO-Z.00	pu	CZ	15
96	VI_PCLK		SDMMC2.B-SCLK	VI-CLK		GPIO-T.00	pd	LV	15
97	SDMMC1_DAT3	SDMMC1-DAT3		UART5.A-TXD		GPIO-Y.04	pu	CZ	15
97	VI_D5		SDMMC2.B-DAT3	VI-D5		GPIO-L.03	pd	LV	15
98	SDMMC1_CMD	SDMMC1-CMD				GPIO-Z.01	pu	CZ	15
98	VI_D1		SDMMC2.B-CMD	VI-D1		GPIO-D.05	pd	LV	15
99	LCD_WR_N	LCD0-SC1	LCD1-SC1	SPI5.B-SCK		GPIO-Z.03	pu	ST	100
99	GMI_WR_N - Gated								
100	SPI1_SCK	SPI2.E-SCK	SPI1.B-SCK		GMI-A26	GPIO-X.05	pu	ST	100

X1 Pin	Tegra Pin Name	Primary Function	Alt 1	Alt 2	Alt 3	GPIO	Reset state	Pad Type	Pull Res. [KOhm]
101	SDMMC1_DAT0	SDMMC1-DAT0		UART5.A-RTS_N		GPIO-Y.07	pu	CZ	15
101	VI_D2		SDMMC2.B-DAT0	VI-D2		GPIO-L.00	pd	LV	15
102	SPI1_CS0_N	SPI2.E-CS1_N	SPI1.B-CS0_N		GMI-A27	GPIO-X.06	pu	ST	100
103	SDMMC1_DAT1	SDMMC1-DAT1		UART5.A-CTS_N		GPIO-Y.06	pu	CZ	15
103	VI_D3		SDMMC2.B-DAT1	VI-D3		GPIO-L.01	pd	LV	15
104	SPI1_MISO		SPI1.B-MISO			GPIO-X.07	pd	ST	100
105	GMI_CS4_N		NAND-CE2_N	GMI-CS4_N		GPIO-K.02	pu	ST	100
106	GMI_CS3_N		NAND-CE1_N	GMI-CS3_N	GMI-INT1	GPIO-K.04		ST	100
107	GMI_CS2_N		NAND-CE0_N	GMI-CS2_N		GPIO-K.03		ST	100
110	GPIO_PU2		UART1.B-CTS_N	GMI-A8		GPIO-U.02	z	ST	100
111	UART2_RTS_N	UART1.C-TXD	UART2-RTS_N	GMI-A0	SPI4.B-MISO	GPIO-J.06	pu	ST	100
112	GPIO_PU3	PWFM-PWM0	UART1.B-RTS_N	GMI-A9		GPIO-U.03	z	ST	100
113	UART2_CTS_N	UART1.C-RXD	UART2-CTS_N	GMI-A1	SPI4.B-CS1_N	GPIO-J.05	pu	ST	100
114	GPIO_PU4	PWFM-PWM1	UART1.B-DTR_N	GMI-A10		GPIO-U.04	z	ST	100
115	UART3_TXD	UART3-TXD		GMI-A2		GPIO-W.06	pu	ST	100
116	GPIO_PU5	PWFM-PWM2	UART1.B-RI_N	GMI-A11		GPIO-U.05	z	ST	100
117	UART3_RXD	UART3-RXD		GMI-A3		GPIO-W.07	pu	ST	100
118	GPIO_PU6	PWFM-PWM3	UART1.B-DSR_N	GMI-A12		GPIO-U.06	z	ST	100
119	UART3_RTS_N	UART3-RTS_N	PWFM-PWM0	GMI-A4		GPIO-C.00	pu	ST	100
120	DAP4_FS	I2S3-LRCK		GMI-A13		GPIO-P.04	pd	ST	100
121	UART3_CTS_N	UART3-CTS_N		GMI-A5		GPIO-A.01	pu	ST	100
122	DAP4_DIN	I2S3-SDATA_IN		GMI-A14		GPIO-P.05	pd	ST	100
123	GPIO_PU0	OWR-PCTLZ	UART1.B-TXD	GMI-A6		GPIO-U.00	z	ST	100
124	DAP4_DOUT	I2S3-SDATA_OUT		GMI-A15		GPIO-P.06	pd	ST	100
125	GPIO_PU1		UART1.B-RXD	GMI-A7		GPIO-U.01	z	ST	100
126	GMI_CS0_N		NAND-CE6_N	GMI-CS0_N	DTV-PSYNC_ERROR	GPIO-J.00	pu [5]	ST	100
127	GEN2_I2C_SDA	I2C2-DAT		GMI-CS7_N		GPIO-T.06	z	DD	50
128	GMI_CS1_N		NAND-CE7_N	GMI-CS1_N	DTV-CLK	GPIO-J.02	pu	ST	100
129	SPI2_CS1_N		SPI2.B-CS1_N			GPIO-W.02	pu	ST	100
130	GMI_CS6_N	NAND-BSY1	NAND-CE4_N	GMI-CS6_N	SATA-ACTIVE	GPIO-I.03	pu	ST	100
131	SPI2_CS2_N		SPI2.B-CS2_N			GPIO-W.03	pu	ST	100
132	GMI_CS7_N	NAND-BSY2	NAND-CE5_N	GMI-CS7_N	GMI-RST_N	GPIO-I.06	pu	ST	100
133	GEN2_I2C_SCL	I2C2-CLK		GMI-CS6_N		GPIO-T.05	z	DD	50
134	SPI1_MOSI	SPI2.E-MOSI	SPI1.B-MOSI		GMI-A25	GPIO-X.04	pu	ST	100
135	ACC1_DETECT	ACC1_DETECT							0
135	SPDIF_IN	SPDIF1.A-IN	HDA.B-RESET		SDMMC2.C-DAT3	GPIO-K.06	pu	ST	50
136	SPI2_CS0_N	SPI6-CS0	SPI2.B-CS0_N		GMI-A24	GPIO-X.03	pu	ST	100
136	LCD_D18	LCD0-HP1	LCD1-HP1			GPIO-M.02	pd	ST	100
137	USB1_VBUS	USB1_VBUS							0
137	SPDIF_OUT	SPDIF1.A-OUT			SDMMC2.C-DAT2	GPIO-K.05	pu	ST	50
138	SPI2_SCK	SPI6-SCK	SPI2.B-SCK		GMI-A23	GPIO-X.02	pu	ST	100
138	LCD_D19	LCD0-HP2	LCD1-HP2			GPIO-M.03	pd	ST	100
139	USB3_DP	USB3_DP							0
140	SPI2_MISO	SPI6-MISO	SPI2.B-MISO		GMI-A22	GPIO-X.01	pd	ST	100
140	LCD_D20	LCD0-VP1	LCD1-VP1			GPIO-M.04	pd	ST	100
141	USB3_DN	USB3_DN							0
142	SPI2_MOSI	SPI6-MOSI	SPI2.B-MOSI		GMI-A21	GPIO-X.00	pd	ST	100
142	LCD_D21	LCD0-HP0	LCD1-HP0			GPIO-M.05	pd	ST	100
143	USB1_DP	USB1_DP							0
144	DAP2_DOUT	I2S1-SDATA_OUT	HDA.B-SDO		GMI-A20	GPIO-A.05	pd	ST	100
144	LCD_D22	LCD0-DI	LCD1-DI			GPIO-M.06	pd	ST	100
145	USB1_DN	USB1_DN							0
146	DAP2_DIN	I2S1-SDATA_IN	HDA.B-SDI		GMI-A19	GPIO-A.04	pd	ST	100
146	LCD_D23	LCD0-PP	LCD1-PP			GPIO-M.07	pd	ST	100
149	GMI_AD0		NAND-D0	GMI-AD00		GPIO-G.00	z	ST	100
150	GMI_ADV_N		NAND-ALE	GMI-ADV_N		GPIO-K.00	1 [4]	ST	100
151	GMI_AD1		NAND-D1	GMI-AD01		GPIO-G.01	z	ST	100
152	GMI_CLK		NAND-CLE	GMI-CLK		GPIO-K.01	0 [4]	ST	100
152	OWR	OWR-IO	CEC-IO				z	OD	
153	GMI_AD2		NAND-D2	GMI-AD02		GPIO-G.02	z	ST	100
154	LCD_PWR0	LCD0-PW0	LCD1-PW0	SPI5.B-MOSI		GPIO-B.02	pd	ST	100
155	GMI_AD3		NAND-D3	GMI-AD03		GPIO-G.03	z	ST	100
156	LCD_SDIN	LCD0-SDI	LCD1-SDI	SPI5.A-MISO		GPIO-Z.02	pu	ST	100
157	GMI_AD4		NAND-D4	GMI-AD04		GPIO-G.04	z	ST	100
158	LCD_SDOUT	LCD0-SDA	LCD1-SDA	SPI5.A-MOSI		GPIO-N.05	pu	ST	100
159	GMI_AD5		NAND-D5	GMI-AD05		GPIO-G.05	z	ST	100
160	LCD_CS0_N	LCD0-CS_N	LCD1-CS_N	SPI5.A-CS2_N		GPIO-N.04	pu	ST	100
161	GMI_AD6		NAND-D6	GMI-AD06		GPIO-G.06	z	ST	100
162	LCD_DC0	LCD0-DC	LCD1-DC			GPIO-N.06	pd	ST	100
163	GMI_AD7		NAND-D7	GMI-AD07		GPIO-G.07	z	ST	100
164	LCD_SCK	LCD0-SCK	LCD1-SCK	SPI5.A-SCK		GPIO-Z.04	pu	ST	100
165	GMI_AD8	PWFM-PWM0	NAND-D8	GMI-AD08		GPIO-H.00	pd	ST	100
166	GPIO_PBB4	VI.A-VGP4	LCD0.C-HSYNC	LCD1.C-HSYNC	SDMMC4.B-DAT4	GPIO-BB.04	z	ST	50

X1 Pin	Tegra Pin Name	Primary Function	Alt 1	Alt 2	Alt 3	GPIO	Reset state	Pad Type	Pull Res. [KOhm]
167	GMI_AD9	PWFM-PWM1	NAND-D9	GMI-AD09		GPIO-H.01	pd	ST	100
168	GPIO_PBB5	VI.A-VGP5	LCD0.C-VSYNC	LCD1.C-VSYNC	SDMMC4.B-DAT5	GPIO-BB.05	z	ST	50
169	GMI_AD10	PWFM-PWM2	NAND-D10	GMI-AD10		GPIO-H.02	pd	ST	100
170	GPIO_PBB6	VI.A-VGP6	LCD0.C-PCLK	LCD1.C-PCLK	SDMMC4.B-DAT6	GPIO-BB.06	z	ST	50
171	GMI_AD11	PWFM-PWM3	NAND-D11	GMI-AD11		GPIO-H.03	pd	ST	100
172	GPIO_PBB7	I2S4.A-SDATA_OUT			SDMMC4.B-DAT7	GPIO-BB.07	z	ST	50
173	GMI_AD12		NAND-D12	GMI-AD12		GPIO-H.04	z	ST	100
174	DAP1_FS	I2S0-LRCK	HDA.A-SYNC	GMI-D28	SDMMC2.C-CMD	GPIO-N.00	pd	ST	50
175	GMI_AD13		NAND-D13	GMI-AD13		GPIO-H.05	z	ST	100
176	DAP1_DIN	I2S0-SDATA_IN	HDA.A-SDI	GMI-D29	SDMMC2.C-DAT0	GPIO-N.01	pd	ST	50
177	GMI_AD14		NAND-D14	GMI-AD14		GPIO-H.06	z	ST	100
178	DAP1_DOUT	I2S0-SDATA_OUT	HDA.A-SDO	GMI-D30	SDMMC2.C-DAT1	GPIO-N.02	pd	ST	50
179	GMI_AD15		NAND-D15	GMI-AD15		GPIO-H.07	z	ST	100
180	DAP1_SCLK	I2S0-SCLK	HDA.A-BCLK	GMI-D31	SDMMC2.C-SCLK	GPIO-N.03	pd	ST	50
184	DAP2_SCLK	I2S1-SCLK	HDA.B-BCLK		GMI-A18	GPIO-A.03	pd	ST	100
186	DAP2_FS	I2S1-LRCK	HDA.B-SYNC		GMI-A17	GPIO-A.02	pd	ST	100
188	DAP4_SCLK	I2S3-SCLK		GMI-A16		GPIO-P.07	pd	ST	100
190	GPIO_PCC1	I2S4.A-LRCK			SDMMC4.B-CMD	GPIO-CC.01	pu	ST	50
190	KB_ROW11	KBC-ROW11	NAND_D11	SDMMC2.A-CMD		GPIO-S.03	pd	ST	50
192	GPIO_PBB0	I2S4.A-SDATA_IN			SDMMC4.B-DAT0	GPIO-BB.00	z	ST	50
192	KB_ROW12	KBC-ROW12	NAND_D12	SDMMC2.A-DAT0		GPIO-S.04	pd	ST	50
194	GEN1_I2C_SDA	I2C1-DAT				GPIO-C.05	z	DD	50
196	GEN1_I2C_SCL	I2C1-CLK				GPIO-C.04	z	DD	50

1) After reset, the default settings of the pull up/down resistor are contrarian. In order to define the logical level, an additional external 47kOhm pull up resistor is placed.
2) This pin features an additional external pull up resistor (94kOhm). For more information about this pin see also the chapter “Recovery Mode”
3) This pin works as reset output for the baseboard. The pin is driven low during reset of the Tegra. Afterwards, it goes high (see section 5.1.3). The pin features an additional external pull up resistor (10kOhm).
4) Pin state is "z" with input enabled, until shortly after SYS_RESET_N goes inactive (high) at which point, the state transitions to listed POR pin state
5) Pin state is "1" (driven high) or "pu" (weak internal Pull-up) when SYS_RESET_N is low. After SYS_RESET_N goes inactive (high) the pin transitions to listed POR pin state

5. Interface Description

5.1 Power Signals

5.1.1 Digital Supply

Table 5-1 Digital Supply Pins

X1 Pin #	Signal Name	I/O	Description	Remarks
42, 84,108, 148,182,198, 200	3V3	I	3.3V main power supply	Use decouples capacities on all pins.
39, 41, 83, 109,147, 181, 197, 199	GND	I	Digital Ground	
40	VCC_BATT	I/O	RTC Power supply can be connected to a backup battery.	Connect this pin to 3.3V even the internal RTC is not used.

5.1.2 Analog Supply

Table 5-2 Analog Supply Pins

X1 Pin #	Signal Name	I/O	Description	Remarks
10, 12	AVDD_AUDIO	I	3.3V analog supply	Connect this pin in any case to a 3.3V supply. For better Audio accuracy we recommend filtering this supply separately from the digital supply. This pin is only connected with the Audio Codec.
9, 11	VSS_AUDIO	I	Analog Ground	Connect this pin in any case to GND. For better Audio accuracy we recommend filtering this supply separate from the digital supply. Internally this pin is connected with Digital GND on the Colibri T30.

5.1.3 Reset

Table 5-3 Reset Pins

X1 Pin #	Signal Name	I/O	Description	Remarks
26	nRESET_EXT	I	Reset Input	This pin is low active and resets the Colibri module. This pin is connected to the power manger IC.
87	nRESET_OUT	O	Reset Output	This pin is active low. This pin is driven low at boot up. There is a 10k Ohm pullup on this pin.

5.2 GPIOs

Most of the pins have a GPIO (General Purpose Input/Output) function. All GPIO pins can be used as interrupt source.

5.2.1 Wakeup Source

Certain pins can be used to wake up the Colibri from a suspended state. There is on-chip deglitch logic, which can be de-activated if required. A signal pulse of at least 46us is recommended to wake up the system. It is possible to choose the wakeup level.

Table 5-4 Wakeup Pins

X1 Pin#	Wakeup Source	Remarks
27	WAKE32	
37	WAKE0	
43	WAKE8	Default Wakeup Source
45	WAKE1	
47	WAKE9	
49	WAKE26; WAKE36	
51	WAKE28	
53	WAKE29	
55	WAKE3	
73	WAKE27	
95	WAKE23	
103	WAKE2; WAKE13	
105	WAKE34	
116	WAKE6	
118	WAKE7	
126	WAKE33	
128	WAKE15	
129	WAKE12	
131	WAKE11	
132	WAKE35	
135	WAKE21	
137	WAKE19	
170	WAKE5	
178	WAKE30	
192	WAKE25	

Additionally, the module can also be waked up by the HOTPLUG_DETECT signal which is located at pin 14 of the additional HDMI/VGA FFC connector X2. The wakeup source of this signal is WAKE4. The touch pen down interrupt signal of the touch controller is connected to the WAKE24 source and can therefore also be used to wake up the system.

5.3 Ethernet

The Colibri Module features a 10/100 Mbit Ethernet interface. The MAC/PHY is already on the Colibri, so you only need the magnetics on your base board.
Please check the datasheet of the Asix AX88772B Ethernet chip to learn more about the Ethernet pins.

5.4 USB

The Colibri T30 provides a USB 2.0 High Speed (480 Mbit/s) port and a USB 2.0 High Speed OTG port. The shared OTG USB Host/Client port can also be used for the USB recovery mode, see the chapter “Recovery Mode” for more information.

5.4.1 USB Data Signal

Table 5-5USB Data Pins

X1 Pin#	Signal Name	I/O	Description
139	USBH_P	I/O	Positive Differential Signal for USB Host port
141	USBH_N	I/O	Negative Differential Signal for USB Host port
143	USBC_P	I/O	Positive Differential Signal for the shared USB Host / Client port
145	USBC_N	I/O	Negative Differential Signal for the shared USB Host / Client port

5.4.2 USB Control Signals

Table 5-6 USB OTG Pins

X1 Pin#	Signal Name	I/O	Description
135	USB_ID	I	Use this pin to detect the ID pin if you use USB OTG
137	USBC_DET	I	Use this pin to detect if VBUS is present (5V USB supply). Please note that this pin is only 3.3V tolerant

If you use the USB Host function you need to generate the 5V USB supply voltage on your base board. The Colibri T30 provides two optional signals for the USB supply. We recommend using the following pins to guarantee the best possible compatibility, however - you can use other GPIOs or not use the signals at all.

Table 5-7 USB Power Control Pins

X1 Pin#	Signal Name	I/O	Description
129	USB_OC	I	USB overcurrent, this pin can Signal an over current condition in the USB supply
131	USBC_PET	O	This pin enables the external USB voltage supply.

5.5 Display

The Colibri T30 has two independent display controllers. Each of the two display controllers shares access to the various output ports. There is only one instance of the parallel LCD, HDMI and TV outputs. Only one display controller can access one of these outputs at any given time. If you are using a smart display (displays with an internal frame-buffer) it is possible to use both display controllers on the parallel display interface.

Features for each display controller

- Three display windows (main frame buffer and 2 overlays)
- Hardware surface blending
- Hardware cursor
- Fully programmable display timing and resolution

5.5.1 Parallel RGB LCD interface

The Colibri T30 provides a parallel LCD interface on the SODIMM connector. It supports up to 24 bit colors per pixel.
The first 18bits are backward compatible with the existing Colibri PXAxxx family. It is also possible to use this interface for a smart display. If you use 18bit or less you can use the other bits for a smart display. However there are only a few special cases where it makes sense to use such a smart display.

Features

- Up to QXGA (2048x1536) resolution
- Up to 24 bit color
- Supports parallel TTL displays and smart displays
- Max pixel clock 165MHz

The following list details the most common color configurations.

Table 5-8 Color Configuration

Tegra Pin Name	24 bit RGB	18 bit RGB	16 bit RGB
LCD_D23	R1		
LCD_D22	R0		
LCD_D21	G1		
LCD_D20	G0		
LCD_D19	B1		
LCD_D18	B0		
LCD_D17	R7	R5	R4
LCD_D16	R6	R4	R3
LCD_D15	R5	R3	R2
LCD_D14	R4	R2	R1
LCD_D13	R3	R1	R0
LCD_D12	R2	R0	
LCD_D11	G7	G5	G5
LCD_D10	G6	G4	G4
LCD_D9	G5	G3	G3
LCD_D8	G4	G2	G2
LCD_D7	G3	G1	G1
LCD_D6	G2	G0	G0
LCD_D5	B7	B5	B4
LCD_D4	B6	B4	B3
LCD_D3	B5	B3	B2
LCD_D2	B4	B2	B1
LCD_D1	B3	B1	B0
LCD_D0	B2	B0	

Table 5-9 Additional Display

X1 Pin#	Signal Name	I/O	Description
44	LCD_DE / LCD_M1	O	Data Enable (other names: Output Enable) For Passive Displays you can use this pin as Bias/Modulation pin
56	LCD_PCLK	O	Pixel Clock (other names: Dot Clock, L_PCLK_WR)
68	LCD_HSYNC	O	Horizontal Sync (other names: Line Clock, L_LCKL_A0)
82	LCD_VSYNC	O	Vertical Sync (other names: Frame Clock, L_FCLK)

Typically you will also require some signals to control the Backlight and/or the Display Enable Signal. You can use any free GPIO for this function but we recommend using the same than we did on our standard base boards, this minimizes the required SW configurations. If you like to use a PWM signal to control the backlight use a pin with PWM function for the Backlight Control, see also chapter 5.11.

5.5.2 HDMI

The HDMI interface is available on the X2 FFC connector on the back of the Colibri T30 module. This interface is compatible with the Colibri T20 module but not backwards compatible with older Colibri PXAxxx modules.

HDMI provides a unified method of transferring both video and audio data over a TMDS compatible physical link to an audio/visual display device.
Please note that the signals HDMI (TMDS) cannot be used as GPIOs.

Features
- HDMI 1.4a up to 1080p60
- Supports digital sound
- High-bandwidth Content Protection (HDCP) with internal SecureROM (license needed)

5.5.3 Analog VGA

The analog VGA interface is also available on the X2 FFC connector on the back of the Colibri T30 module. It supports analog VGA (analog RGB) and S-Video TV out. This interface is compatible with the Colibri T20 module but not backwards compatible with older Colibri PXAxxx modules.

Please contact Toradex if you plan to use the Analog VGA interface.

Features
- Up to WUXGA (1920x1200) resolution

5.5.4 DDC (Display Data Channel)

The Colibri T30 can automatically detect the connected display over the DDC. The DDC port is 5V compatible. DDC is realized with the I^2C Port 4 controller.

5.5.5 LVDS

The Colibri does not have a direct a LVDS interface. However, it is very easy to use the parallel LCD port with an LVDS transmitter. The Colibri Evaluation board provides a reference design for an LVDS interface implementation. Contact Toradex if you have any questions how to connect a LVDS transmitter (e.g 24bit colors).

5.6 External Memory Bus

The Colibri T30 features a 16bit external memory bus. This memory bus is exclusively for your devices, there are no internal chips connected to this bus. This means you can adjust all the settings to optimize the access to your devices.
The memory controller supports the programmed IO mode (PIO) or DMA transfers.

Features

- Supports 16 bus width
- Up to 28 address bits
- Chip select, multiplexed to 8 different pins
- Data ready signal support
- Synchronous and asynchronous access supported
- Multiplexed and de-multiplexed address/data mode

The memory bus is typically used to connect high speed devices like FPGAs, DSPs, additional Ethernet controllers, Wifi chips etc.

5.6.1 Non-Multiplexed Mode

In this mode the address and data signals use different pins. This mode is compatible with all our Colibri modules.

5.6.2 Multiplexed Mode

In the multiplexed mode the data signals are also used to transmit the addresses. This reduces the required number of lines to connect a device. You can use GMI_ADV_N (X1 pin 150) to separate data and addresses. If you use the 16bit mode it is only possible to transfer the lower 16 address bits over the data bus. The upper address lines are on the non-multiplexed address pins. This mode is not compatible with our Colibri PXA270 modules.

5.6.3 External Memory Map

The address space is 256MB large for each Chip Select. You can switch the CS in a special register. See the T30 Technical Reference Manual for more details.

On the Colibri T30 the mapping of the address bit than same than on the Colibri T20 but it is different than on the Colibri PXAs.
The external address pin A[0] correlates to the internal memory address bit 1, external address pin A[1] to internal memory address bit 2, and so on.

5.6.4 Memory Bus Signals

Table 5-10 Address and Data Pins

X1 Pin #	Compatible Function	Tegra Memory Bus Function	I/O	Description
116,114,112,110, 125,123,121,119, 117,115,113,111	Address[11:0]	GMI_A[11:0]	O	Non-Multiplexed address bits 0 to 11. They are compatible with all Colibri modules.

X1 Pin #	Compatible Function	Tegra Memory Bus Function	I/O	Description
134,136,138,140, 142,144,146,184, 186,188,124,122, 120,118	Address[25:12] only Colibri PXA270	GMI_A[25:12]	O	Non-Multiplexed address bits 12 to 25. This pin functions are not with all Colibri Modules compatible. See the Toradex Colibri Migration Guide for more information Multiplexed Mode: In the 16bit mode the bits 16:25 are the non-multiplexed address bits.
102, 100	-	GMI_A[27:26]	O	Non- Multiplexed Address bits 26 and 27. This pin functions are not available on the Colibri PXAxx family. Multiplexed Mode: In the 16bit mode the bits 26 and 27 are the non-multiplexed address bits.
179,177,175,173, 171,169,167,165, 163,161,159,157, 155,153,151,149	Data[15:0]	GMI_AD[15:0]	I/O	Non- Multiplexed Mode: Data bits 0 to 15 Multiplexed Mode: Data/Address bits 0 to 15 The Non-Multiplexed Function is compatible with all modules GMI_AD[3:0] are with 100kOhm pulled up. GMI_AD[7:4] are with 100kOhm pulled down.

Note: Please see the table in chapter 4.4 for more information

Table 5-11 Bus Control Signals

X1 Pin #	Compatible Function	Tegra Memory Bus Function	I/O	Description
89	nWE	GMI_WR_N	O	Write Enable
91	nOW	GMI_OE_N	O	Output Enable Pulled up on the Colibri with 54 kOhm. This pin is also used for the Recovery Mode. For more information see the “Recovery Mode” chapter.
93	RDnWR	GMI_WR_N	O	The Tegra chip does not provide an RDnWR function. We routed GMI_WR_N to this pin (through a buffer). (GMI_WR_N is also available on X1 pin 89) . The GMI_WR_N provides a similar function than the RDnWR function, however the timing is a little different. This pin is multiplexed with another pin, please chapter 4.1 for more information
95	RDY	GMI_WAIT GMI_IORDY	I	Wait (or Ready): Level configurable input. When asserted, WAIT (RDY) indicates the read data is invalid (Wait) or Valid (Ready). Typically used for variable latency IOs. This pin is multiplexed please check chapter 4.1 for more information
99	(nPWE)	GMI_WR_N	O	Write Enable This is the same signal than on pin 89. Except that the signal passes a buffer. Pin SDMMC3_DAT4 is used to tristate the buffer, see the **Error! Reference source not found.** in chapter 4.1 For new carrier board designs use Pin 89 for this functionality and \ tristate the buffer to Pin 99.
47,105, 106, 107, 126, 128, 130, 132	nCS and others	GMI_CSx_N	O	Chip Select Signals We recommend to use the CS signals on the pins X1 105, 106, 107 due compatibility to our other Colibri modules. Please see the Colibri Migration Guide for more information
150	-	GMI_ADV_N	O	Address Valid This signal is used for muxed operations For synchronous read operations, the address is typically latched either on the edge active -> inactive of ADV_N or on the first rising edge of CLK after ADV_N goes active (slow devices <= 108MHz) or on the last rising edge of CLK after ADV_V goes active (faster devices >= 108MHz) For asynchronous reads, the address is latched on the edge active -> inactive of ADV_N. For writes, ADV_N is held active and

X1 Pin #	Compatible Function	Tegra Memory Bus Function	I/O	Description
				the address is valid throughout the cycle for non-muxed operation. In the non-muxed case the address will be valid for the duration of the entire access. Only in the muxed modes is it valid during the ADV_N (minimum 2 cycles) This signal is with 100kOhm pulled down.
152	-	GMI_CLK	O	Clock, used to synchronize the Colibri and the device during Synchronized accesses. Rising edge active. This signal is with 100kOhm pulled down.

Note: Please see the table in chapter 4.4 for more information

5.7 IDE

The Colibri T30 does not support an IDE interface.

5.8 I²C

The Colibri T30 offers five I²C controllers. They implement the I²C 2.1 specification. All can be used as master or slave. Port 0 is used for power management and is not available externally. Port 4 is typically used for DDC and is only available on the extension connector X2 for more information see Table 3.2.2.

Features:

- Supports standard and fast mode of operation (0-400KHz) as well as high speed mode (3.4 MHz).
- Independent Master Controller and Slave Controller
- Master supports clock stretching by the slave
- Supports one to eight-byte burst data transfers
- 7-bit or 10-bit addressing
- Fully programmable 7-bit or 10-bit address for the slave
- Supports general call addressing
- Supports Recognition and Transfer of data to peripherals that do not send an acknowledge
- Master supports packet based DMA
- Supports 4kByte of transfer in packet mode (can be extended by using multiple packets)
- Clock Low Timeout (SMB Bus)

There are a lot of low speed devices which use I²C interfaces such as RTCs or sensors but it is also used to configure other devices like cameras or displays. The I2C Bus is also used to communicate with SMB Bus devices.

Table 5-12 I²C Signals

X1 Pin #	Compatible Function	Tegra Pin Name	I²C Port	Description
194	I2C_SDA	GEN1_I2C_SDA	1	Tegra I²C port 1 Data (Recommended Pin for I²C)
196	I2C_SCL	GEN1_I2C_SCL	1	Tegra I²C port 1 Clock (Recommended Pin for I²C)
127	EXT_IO2(GPIO)	GEN2_I2C_SDA	2	Tegra I²C port 2 Data
133	EXT_IO1(GPIO)	GEN2_I2C_SCL	2	Tegra I²C port 2 Clock
51	MMC_DAT2	CAM_I2C_SDA	3	Tegra I²C port 3 Data
49	MMC_DAT1	CAM_I2C_SCL	3	Tegra I²C port 3 Clock

For more configurations see the table in chapter 4.4

5.9 UART

The Colibri Tegra provides up to five serial UART interfaces. Three of them are backward compatible with the Colibri T20 and PXAxxx modules. UART2 (provided by default on the STD_UART pins) can be used as VFIR (Very Fast Infra-Red) interface.

UART Features

- Support 16450 and 16550 compatible modes
- 16 byte FIFO
- Up 4 Mbaud
- Word length 5 to 8 bit, optional parity, one or two stop bits
- Auto sense baud detection

VFIR Features

- Supports up to IrDA version 1.4 with 16Mbit/s
- 32bit x 16 deep FIFO

5.10 SPI

The Tegra chip has 6 SPI controllers from which you can use maximal 5 at the same time. They operate at up to 35 Mbps and provide full duplex, synchronous, serial communication between the Colibri module and external peripheral devices. Each SPI channel consists of four signals; clock, chip select (frame), data in and data out. In the Nvidia Datasheets SPI is also called SLINK.

Features:

- Up to 35 Mbps
- 32bit x 32 deep FIFO
- Packet size 1-32 bit
- Packed mode with 8 or 16bit packet size
- Receive compare mode where the controller checks for a particular pattern in the incoming data stream before transferring the data to the FIFO
- Simultaneous receive and transmit

Each SPI channel supports four different modes of the SPI protocol:

Table 5-13 SPI Modes

SPI Mode	Clock Polarity	Clock Phase	Description
0	0	0	Clock is positive polarity and the data is latched on the positive edge of SCK
1	0	1	Clock is positive polarity and the data is latched on the negative edge of SCK
2	1	0	Clock is negative polarity and the data is latched on the positive edge of SCK
4	1	1	Clock is negative polarity and the data is latched on the negative edge of SCK

SPI can be used as a fast interface for ADCs, DACs, FPGAs, etc. Some LCD displays require to be configured over SPI prior to being driven via the RGB or LVDS interface.

Table 5-14 Backwards Compatible SPI Signals

X1 Pin #	Compatible Function	Tegra Memory SPI Function	I/O	Description
86	SSPFRM	SPI1_CS0_N	I/O	SPI Chip Select/ SPI Frame/ SPI Enable Signal
88	SSPSCLK	SPI1_SCK	I/O	SPI Clock
90	SSPRXD	SPI1_MISO	I/O	SPI Master Input / Slave Output
92	SSPTXD	SPI1_MOSI	I/O	SPI Master Output / Slave Input

For a list with more SODIMM pins with SPI functions have a look at the table in chapter 4.4

5.11 PWM (Pulse Width Modulation)

The Colibri T40 features a four channel Pulse Width Modulator (PWM). The duty cycle has an 8 bit resolution (that is, it can be set to a value of between 0 and 255 in steps of 1/256). The maximum frequency output is 187.5 kHz.

The PWM interface can be used as an easy way to emulate a DAC and generate a variable DC voltage if used with a suitable RC circuit. Other uses include control of LED brightness, display backlights or servo motors.

5.12 OWR (One Wire)

The One Wire Controller (OWR) implements a device communications bus system that provides low-speed data, signaling and power over a single signal. The OWR uses two signals for this - one for ground, and the other for power and data.
On the Colibri T30 the one wire protocol is primarily intended for communication with battery controller chips.

Features

- FIFO depth of 32 x 32 bits
- Hard-wired implementation of one wire protocol to eliminate need for external bridge chip
- 1 MHz device clock required
- Supports de-glitch
- Supports Byte transfer or 1 Bit transfer
- Supports the following commands: Read Rom, Skip Rom, Read Mem, Read Status, Read Data/Generate 8 bit CRC, Write Memory, Write Status
- Supports CRC 8/16 bit implementation
- Supports different battery devices, up to a memory size of 256KB in byte transfer
- Generic controller support with device Maxim DS2784

5.13 SD/MMC

The Tegra 3 provides 4 SDIO interfaces, one is used internally for the eMMC Flash the other 3 are available on the SODIMM Pins. The interfaces are capable of interfacing with SD Memory

Cards, SDIO, MMC, CE-ATA cards and eMMC devices. The controllers can acts as both master and slave simultaneously.
The interfaces provide up to 4 data signals.

Features

- Supports SD Memory Card Specification 3.0
- Supports SDIO Card Specification Version 3.0
- Supports addressing larger capacity SD 3.0 or SD-XC cards up to 2 TByte
- Support SPI mode
- Up to 200Mbits per second data rate using 4 parallel data lines (SD 4-bit mode) at 50 MHz
- The IO voltage is 3.3V on the SODIMM pins.

Tegra SDIO interface	Max Bus Width	Recommended Port	Description
1	4bit	common	Shares pins with camera interface
2	4bit	Port A or C	**Standard Interface**
3	4bit	common	Shard with Camera Interface, PWM
4	8bit	N/A	Connected to internal eMMC. Not not use it on the SODIMM Pin

5.14 Analog Audio

The Colibri T30 offers Analog Audio input and output channels.
On the Colibri T30 a Freescale SGTL5000 chip handles the analog audio interface. The SGTL5000 is connected over I2S with the Tegra chip. You can consult the Freescale SGTL5000 datasheet for more information.

Table 5-15 Audio Interface Pins

X1 Pin #	Signal Name	I/O	Description	Pin on the SGTL5000 (20pin QFN)
1	MIC_IN	Analogue Input	Microphone input	10
3	MIC_GND	Analogue Input	Microphone pseudo-ground Possible to connect the GND	(GND or open)
5	LINEIN_L	Analogue Input	Left Line Input	9
7	LINEIN_R	Analogue Input	Right Line Input	8
13	HEADPHONE_GND	Analogue Output	Headphone pseudo-ground	2
15	HEADPHONE_L	Analogue Output	Headphone Left Output	2
17	HEADPHONE_R	Analogue Output	Headphone Right Output	1

5.15 Touch Panel Interface

The Colibri T30 offers a 4-wire touch resistive touch interface.

A ST Microelectronics STMPE811 provides the touch interface. The Microelectronics STMPE811is via I2C connected with the Tegra chip.
Please consult the Microelectronics STMPE811 documentation for more information.

Table 5-16 Touch Interface Pins

X1 Pin #	Signal Name	I/O	Description	Pin on the STMPE811
14	TSPX	Analogue Input	X+ (4-wire)	13
16	TSMX	Analogue Input	X- (4-wire)	16
18	TSPY	Analogue Input	Y+ (4-wire)	15
20	TSMY	Analogue Input	Y- (4-wire)	1

5.16 Analog Inputs

A ST Microelectronics STMPE811 provides the 4 analogue input channels. Please consult the ST Microelectronics STMPE811 documentation for more information.
All AD inputs are protected with a 10k Ohm series resistor between the SODIMM pins and the ADC.

Table 5-17 Analog Inputs Pins

X1 Pin #	Signal Name	I/O	Description	Pin on the STMPE811
2	AD3	Analogue Input	ADC input (3.3V max).	12
4	AD2	Analogue Input	ADC input (3.3V max)	11
6	AD1	Analogue Input	ADC input (3.3V max). The ADC pin is pulled to GND (10k Ohm) for 6µs while booting.	9
8	AD0	Analogue Input	ADC input (3.3V max)	8

5.17 Camera Interface

The Video Capture and Imaging Subsystem (VI) can receive data from TV decoder chips, CMOS sensors and other devices. It supports advanced processing features with its multi-stage pipeline, from lens correction through to color space conversion.
Among other functions, this subsystem removes common artifacts of digital CMOS image sensors and lenses from the raw data, and interpolates alternating, one-color-per-pixel Bayer-formatted data into full RGB color signals.
All of the camera interface pins are multiplexed with other Tegra pins. If you use the camera interface make sure the multiplexed pins are tristated. Additional information can be found in chapter 4.1: Function Multiplexing.

Features

- Raw (Bayer), RGB, YUV input up to 12 Megapixels
- 8/10/12bit parallel video interface
- ITU-R 8bit
- Max pixel clock input 120 MHz
- Max Master clock output (Camera input clock) 80MHz

Table 5-18 Camera Interface Pins

X1 Pin #	Compatible Function	Tegra Pin Name	I/O	Description
75	CIF_MCLK	VI_MCLK	O	Master Clock: Connect to Reference clock input on camera(s)
96	CIF_PCLK	VI_PCLK	I	Pixel Clock: Connect to Pixel CLK input on camera(s)
81	CIF_FV	VI_VSYNC	I	Vertical Sync: Connect to Vsync on camera(s)
97	CIF_LV	VI_HSYNC	I	Horizontal Sync: Connect to Hsync on camera(s)
	CIF_DD[9:0]	VI_D[9:0]	I	Pixel Data bits 0 -9: Connect to Data pins on camera(s).
69	SCL2 (PS2 Keyboard GPIO)	VI_D10	I	Pixel Data bit 10: Connect to a Data pin on camera(s). This data bit is NOT compatible with the complete Colibri family
77	-	VI_D11	I	Pixel Data bit 11: Connect to a Data pin on camera(s). This data bit is NOT compatible with the complete Colibri family

Table 5-19 Camera to Colibri Pin Mapping

Format	Camera Pins	Colibri Pin
YUV	D[7:0]	CIF_DD[9:2]
Bayer 8-bit	D[7:0]	CIF_DD[9:2], connect CIF_DD[1:0] with GND
Bayer 10-bit	D[9:0]	CIF_DD[9:0]

5.18 S/PDIF (Sony-Philips Digital Interface I/O)

The S/PDIF interface supports both input and output of the serial audio digital interface format. The input controller can digitally recover a clock from the received stream. The controller conforms to the AES/EBU IEC 60958 standard. This controller is also used for the audio HDMI output.

Features

- Supports 5 data formats
  - 16-bit
  - 20-bit
  - 24-bit
  - Raw
  - 16-bit packed

- Supports “autolock” mode to automatically detect “spdifin” sample rate and lock onto the data stream.
- Supports override mode to provide a manual control to sample “spdifin” data stream.

5.19 I2S

5.19.1 AC97

The Colibri T30 does not support AC97

5.19.2 I2S

The I2S can be used to connect an additional external audio codec.

Features

- PCM, Network and TDM mode Support
- Master or Slave
- Supports I2S, RJM, LJM and DSP mode data formats
- Maximum device clock of 24 MHz

5.20 Clock Output

The Colibri T30 provides an external Clock on SODIMM (X1) Pin 75.

Available Clock Frequencies: TBD

Care must be taken when changing PLL frequencies; these PLLs are also used internally in the Tegra processor.

5.21 Keypad

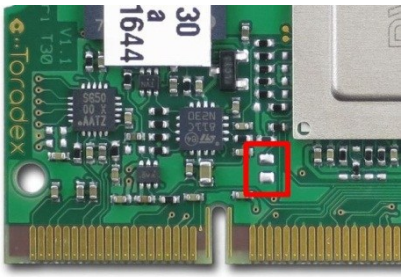
You can use any free GPIOs to realize a Matrix keypad interface.

5.22 JTAG

There is a JTAG interface available on PCB testpoints. On the Evaluation Board 3.1 the signals are accessible through pogo pins. The reference voltage is 3.3V, so the jumper JP 29 must be in position 2-3.
A JTAG interface is not required to work with the Colibri T30. You are always able to reprogram the module via Recovery Mode.

6. Recovery Mode

The shared USB Client/Host port can be used to download new software. This is normally only required if the Bootloader does not boot anymore.
To enter the recovery mode, either connect the recovery mode pads on the front of the module together (see picture below) or pull SODIMM pin 91 to GND with a 10KOhm resistor while booting.



When the module is in recovery mode, the NVFlash tool can be used to re-program the module.

You can find additional information in our Developer Center: http://developer.toradex.com

7. Bootstrap Options

By default the system boots form the internal eMMC card.
Strap pin options: TBD

8. Suspend

In the suspend state the CPU is powered off but the RAM is still powered. It is very fast to wake up form this state.
You can use several pins as Wakeup Sources, see chapter 5.2.1 for more information about possible wakeup sources.

For pin behavior see the Nvidia Tegra 3 datasheet.

9. Known Issues

noneTBD

10. Technical Specifications

10.1 Absolut Maximum Rating

Table 10-1 Absolut Maximum Ratings

Symbol	Description	Min	Max	Unit
Vmax_VCC_BATT	RTC Supply	-0.3	5.5	V
Vmax_IO	Most pins with GPIO functions	-0.5	3.63	V
Vmax_3V3	Digital Supply	-0.3	3.63	V
Vmax_AVDD	Analog Supply	-0.3	3.60	V
Vmax_AIN	Analog Input	-0.3	3.9	V
Vmax_USB	USB Voltage	-0.5	TBD	V

10.2 Electrical Characteristics

TBD

Table 10-2 Typical Power Consumption

Symbol	Description (VCC=3.3V)	Typ	Unit
IDD_IDL	CPU Idle	TDB	mA
IDD_HIGHCPU	Maximal CPU Load	TBD	mA
IDD_HD	Full HD Video on HDMI	TBD	mA
IDD_SUSPEND	Module in Suspend State	TBD	mA

10.3 Power Up Ramp Time Requirements

TBD

10.4 Mechanical Characteristics

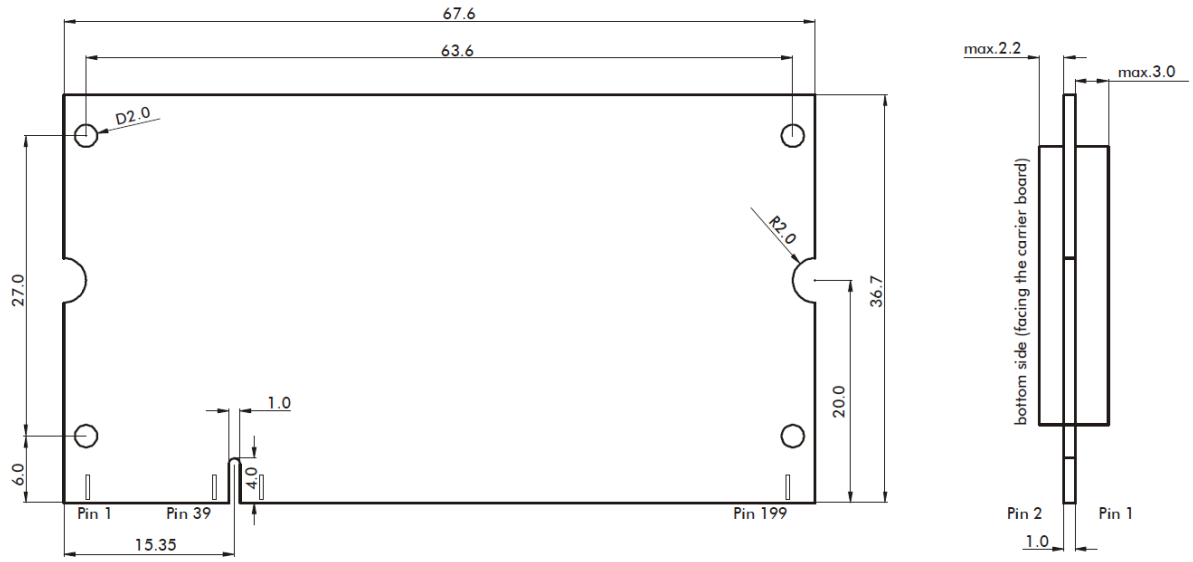


Figure 5 Mechanical dimensions of the Colibri modules
Tolerance for all measures: +/- 0.1mm

10.4.1 Sockets for the Colibri Modules

The Colibri modules fit into a regular 2.5V (DDR1) SODIMM200 memory socket.
A choice of SODIMM200 socket manufacturers is given below:

Admatec GmbH:	http://www.admatec.de/
AUK Connectors:	http://www.aukconnector.com/
CONCRAFT:	http://www.concraft.com.tw/d-DDR.html
Morethanall Co Ltd.:	http://www.morethanall.com/
Tyco Electronics (AMP):	http://www.tycoelectronics.com
NEXUS COMPONENTS GmbH	http://www.nexus-de.com

10.5 Thermal Specification

The Colibri T30 incorporates DVFS (Dynamic Voltage and Frequency Switching) and Thermal Throttling which enables the system to continuously adjust operating frequency and voltage in response to changes in workload and temperature. This allows the Colibri T30 to deliver higher performance at lower average power consumption compared to other solutions.
The Colibri T30 modules come with 2 temperature sensors, one which measures the temperature of the CPU die and another on the Colibri PCB.
In the event that the temperature of the T30 reaches the maximum permitted temperature limit, the system shuts automatically down.

Here some general considerations:
- If you need the full CPU/Graphics performance over a long period of time, we recommend adding a heat solution.
- If you only use the peak performance for a short time period, heat dissipation is less of a problem because the advanced power management reduces power consumption when full performance is not required.

- A lower die temperature will also lower the power consumption due to smaller leakage currents.

In general, the more effective the thermal solution is as dissipating hear, the more performance you can get out of the Colibri T30 Module.

Table 10-3 1.1 Thermal Specification

Module	Description	Min	Typ	Max	Unit
Colibri T30	Operating temperature range	TBD		TBD	°C
Colibri T30	Storage Temperature	TBD		TBD	°C
Colibri T30	Operation temperature as sensed form Thermal Diode	-20		90	°C
	Thermal Design Power at max Temperature Tegra Chip and DDR RAM		TBD		
Colibri T30	Thermal Resistance Junction-to-Ambient, Tegra Chip only. (Theta-JA) [1]		11.6		°C/W
Colibri T30	Thermal Resistance Junction-to-Case, Tegra Chip only. (Theta-JC) [1]		1.18		°C/W
Colibri T30	Thermal Resistance Junction-to-Top of Package, Tegra Chip only, (Psi-JT) [1]		0.89		°C/W

[1] A High K JEDEC Board as defined by JEDEC Standard JESD51-9, Test Boards for Area Array Surface Mount Package Thermal Measurements, was used for thermal modeling to determine thermal performance. Ambient Temp 55 Celsius, No Airflow

10.6 RoHS Compliance

Colibri T30 3 modules comply with the European Union's Directive 2002/95/EC: "Restrictions of Hazardous Substances".