

Course Description

One of the key elements of an electronic system level (ESL) methodology is the concept of platform-based design. When the platform is modeled at a high level of abstraction, it is called "virtual platform". This course shows how the Xilinx Zynq "All Programmable SoC" platform can be abstracted and modeled in a fully functional software representation of a hardware/software SoC design based on a mix of processors (Cortex-A9 dual MPCore and MicroBlaze), software, communication links (AXI interconnects), memories, and other IP cores.

Level – Beginner

Course Duration – 1 day

Price – \$800 or 8 Training Credits

Course Part Number – HDT-VERPRI-100-ILT

Who Should Attend? System architects and software engineers who want to exploit the high performance ARM Cortex-A9 dual MPCore, explore and analyze the impact of different architectures on implementation and determine the best hardware/software partitioning for the Xilinx Zynq "All Programmable SoC" platform.

Prerequisites

- C/C++ knowledge
- Digital design knowledge

Software Tools

- SpaceStudio from Space Codesign Systems Inc.
- Vivado Design Suite from Xilinx Inc.

Hardware

- Zedboard

Lab Descriptions

- Lab 1: Quick overview of an ESL methodology – The objective of this tutorial is to familiarize the student with the different steps of an ESL methodology (i.e., modeling, partitioning, and refinement) by using the SpaceStudio graphical environment to design, simulate and profile a system across different levels of abstraction.
- Lab 2: HW/SW Codesign of a MJPEG application targeting the Zynq platform – At the architectural level using SpaceStudio, given a set of requirements, you will find an optimal hardware/software partitioning for each set. This lab also illustrates how ESL can significantly reduce design time.
- Lab 3: HW/SW Co-Synthesis of a Calculator application – This lab show how to fill the gap between ESL tool (SpaceStudio) and RTL implementation (Vivado) by looking step by step, at how to select and automatically generate all of the required hardware and software code, configuration files and parameters to finally download a system design into a Zedboard.

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Course Outline

- Introduction to Electronic System Level (ESL)
- Levels of abstraction and ESL design flow
- Functional specification and validation in C/C++
- Lab 1 – Quick overview of an ESL methodology
- Zynq platform and its virtualization
- HW/SW Co-design and Architectural Exploration
- Lab 2 – HW/SW Co-design of a MJPEG application targeting the Xilinx Zynq platform
- Refinement of architecture models into an hardware implementation (HW/SW Co-Synthesis)
- Lab 3 – HW/SW Co-Synthesis of a Calculator application
- Advanced Features