Advanced Universal Verification Methodology (UVM)

HDT-ADVUVM-100 (v1.0H)

Course Description

This 3-day workshop class is designed for UVM users who want to take their skills to the next level.

Putting together real world testbenches require more than just knowing the components of the UVM library. Real world testbenches have issues that require knowing how to apply the UVM library to solve these issues. Issues such as multiple interfaces to the DUT, layering stimulus, concurrent process synchronization, dealing with behaviors such as interrupts and multiple response types, and building scalable, reusable testbenches are addressed.

In this Advanced UVM class you will gain experience in dealing with these and other testbench challenges. The class works through various testbench issues and challenges providing solutions. You will be able to apply these solutions to your testbench. You will also take away from this class detailed real world example testbenches that illustrate solutions to issues providing a great reference in doing your testbench.

This class is customized to the needs of the students.

Level – UVM 2

Course Duration – 3 days

Price – $2100

Course Part Number – HDT-ADVUVM-100 (v1.0H)

Who Should Attend? Engineers with UVM experience who want to take their skills to the next level to be able to tackle real world problems.

Prerequisites

- Actual experience with the UVM library or UVM experience in addition to have taken the Introduction to UVM course

Software Tools

- Questa Simulator 10.1a+

After completing this comprehensive training, you will have the necessary skills to:

- Create scalable, reusable UVM testbench structures
- Deal with thorny issues such as reset, interrupts and synchronization across multiple components
- Apply advanced stimulus related techniques such as layered stimulus or complex scenarios
- Apply advanced analysis techniques such as scoreboard draining
- Apply advanced register integration and techniques to your register model

Course Outline

Day 1

- Introduction
- DUT-TB Interface
- Lab - DUT-TB interface
- Container Classes
  - Pools, queues
- Process synchronization
  - Events, barriers, End of Test
- Lab - Synchronization

Day 2

- Advanced phasing
- Lab - Phasing
- Virtual Sequences
  - coordination of multiple interfaces, multiple sequencers
- Lab - Virtual sequences
- Response handling
- Interrupt handling
- Reset

Day 3

- Layered stimulus
- Lab - Layered stimulus
- UVM register model integration
- UVM register Memory Allocation Manager
- Template Method Pattern & UVM Callbacks
- Command line processing
- Emulation considerations
- Coverage driven testing

Hands-On Labs

- A good portion of class time will be spent applying principles learned in lecture to hands-on labs.

Classroom only

- This class is only taught in a classroom setting and not on-line

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