Open Verification Methodology (OVM) Introduction

HDT-OVM-100 (v1.0H)

Course Description

This 4-day course introduces engineers to developing verification environments using the Open Verification Methodology (OVM) library.

The class shows you how to create an OVM testbench structure for your DUT which includes both stimulus generation and analysis. We address how to create test cases that generate stimulus using sequences and SystemVerilog randomization constructs. The class teaches students how to write analysis components such as scoreboards and coverage collectors. You will learn how to create, integrate and use a register model.

Level – OVM 1

Course Duration – 4 days

Price – $2800

Course Part Number – HDT-OVM-100 (v1.0H)

Who Should Attend? Engineers interested in developing SystemVerilog verification environments using the Open Verification Methodology (OVM) library.

Prerequisites

- SystemVerilog for Verification course or equivalent experience using SystemVerilog

Software Tools

- Questa Simulator 10.1a+

After completing this comprehensive training, you will have the necessary skills to:

- Create an OVM testbench structure using the OVM library base classes and the OVM factory
- Declare transaction items types
- Write test cases using sequences to generate stimulus for your DUT
- Develop scoreboards for analysis
- Develop a register model for your DUT and use the model for initialization and accessing DUT registers

Course Outline

Day 1

- Introduction to OVM
- OVM reporting facilities
- Transaction-level communication
- OVM Transactions
- Lab - Transactions
- Testbench components
- Phasing
- Lab - Components
- Start and end of simulation
- Dynamic Construction - Introduction to the OVM Class Factory
- Lab - Test environment

Day 2

- Connecting to the DUT
- Analysis elements
- Scoreboards, coverage collectors, predictors
- Lab - Analysis
- Hierarchy
- Lab - Hierarchy
- Factory Overrides
- Lab - Factory

Day 3

- Configurations
- Lab - configurations
- Introduction to sequences
- Lab - Sequences
- More on sequences
- Lab - Multiple sequences

Day 4

- UVM Registers
  - Register model
  - Register model integration
  - Lab – Register integration
  - Register model use
  - Lab – Register use

Hands-On Labs

- A good portion of class time will be spent applying principles learned in lecture to hands-on labs

Register Today

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