SystemVerilog for Verification

HDT-SYSVER-200 (v1.0H)

Course Description

This 4 day course introduces engineers to developing verification environments using SystemVerilog. The course covers the new basic features in SystemVerilog such as extended data types, array types, extensions to tasks and functions and dynamic processes. The course teaches Object Oriented Program (OOP) modeling using SystemVerilog classes and shows how to create OOP testbenches and connect them to your DUT. New SystemVerilog techniques such as constrained randomization for stimulus generation and covergroups and assertions for analysis are covered as well as how to apply them to your OOP testbench.

Level – SV 1

Course Duration – 4 days

Price – $2800

Course Part Number – HDT-SYSVER-200 (v1.0H)

Who Should Attend? Engineers interested in applying SystemVerilog technology to their verification process.

This course is a prerequisite for engineers interested in learning UVM or OVM.

Prerequisites

- Verilog training or equivalent experience
- For engineers with VHDL experience: Verilog Fundamentals for SystemVerilog course

Software Tools

- Questa Simulator 10.1a+

After completing this comprehensive training, you will have the necessary skills to:

- Use the new data types, array types, and structs in testbenches
- Use dynamic processes to create parallel stimulus
- Create OOP style testbenches using OOP techniques
- Apply SystemVerilog constrained randomization to testbench stimulus generation
- Create covergroups to apply functional coverage to the analysis portion of a testbench
- Create assertions for testing DUT logic
- Bind assertions to a DUT without modifying the DUT
- Go on and learn how to use the Universal Verification Methodology (UVM) library

Course Outline

Day 1

- Introduction to Verification with SystemVerilog
- Language enhancements
  - SystemVerilog Data types
  - Arrays & Structures
  - SV Scheduler
  - Program Control
  - Lab – Sparse memory
  - Hierarchy
  - Tasks & Functions
  - Dynamic Processes
  - Inter-process Sync & Communication
    Lab - Mailboxes

Day 2

- Classes
  - Class basics
  - Constructors
  - Lab - oop
  - Virtual methods
  - Inheritance
  - Parameterization
  - Polymorphism
    Lab - polymorphism

Day 3

- Interfaces
- Lab – Virtual interfaces
- Randomization & Constraints
  - Randomize
  - Constraints
  - Random sequences
  - Lab - Randomization
- Functional Coverage
  - Covergroups
  - Coverpoints and cross
  - Lab - Covergroups

Day 4

- SVA
  - Concurrent assertion basics
  - Lab – Assertion basics
  - Boolean expressions
  - Sequences
  - Lab – Sequences
  - Lab – Data values
  - Properties
  - Verification directives
  - Lab - Bind

Hands-On Labs

A good portion of class time will be spent applying principles learned in lecture to hands-on labs

Register Today

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Email: training@hardent.com
Telephone: 514-284-5252

Course material created by: