

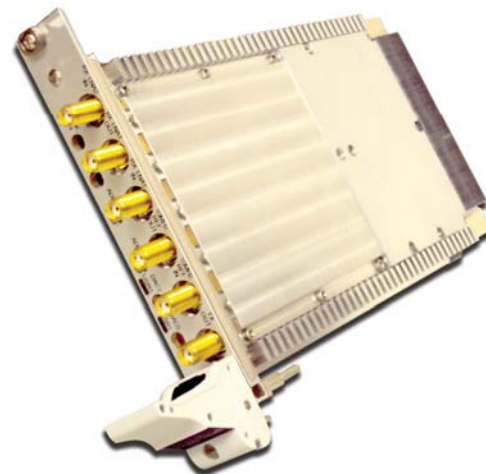
High Linearity Wideband RF-to-Digital Transceiver

RF-7902

Preliminary

Features

- Integrated RF and Digital IF Processing in a single 3U OpenVPX slot
- High linearity, wideband RF Transceiver, 200 MHz to 2.7 GHz
- 14-bit ADC 490 MSPS, 16-bit DAC 980 MSPS
- Fast-frequency hopping up to 3000 hops/sec
- Up to 170 MHz Receiver analog bandwidth
- Up to 400 MHz Transmitter analog bandwidth
- Xilinx Virtex-5 SX95T-2 User FPGA for flexible IF signal processing
- High-speed serial connection to host processor
- Software drivers and API, FPGA interface libraries, and example code included
- Digital Down Converter (DDC) and Digital Up Converter (DUC) IP included
- Rugged conduction- or air-cooled form factors available
- Designed to operate with host SBC, VPX-1131, VPX-1151, and VPX-8320 as part of Spectrum's SDR-7000 family
- Not subject to US ITAR control



Applications

- Wideband Datalinks (eg. UAV, UGV, USV)
- Ground Mobile Communications
- Air-to-Ground Communications
- Communications Electronic Warfare
- SIGINT – COMINT/ELINT
- Satellite Ground Terminals
- Cognitive Radio
- Software Defined Radio (SDR) and Waveform Development

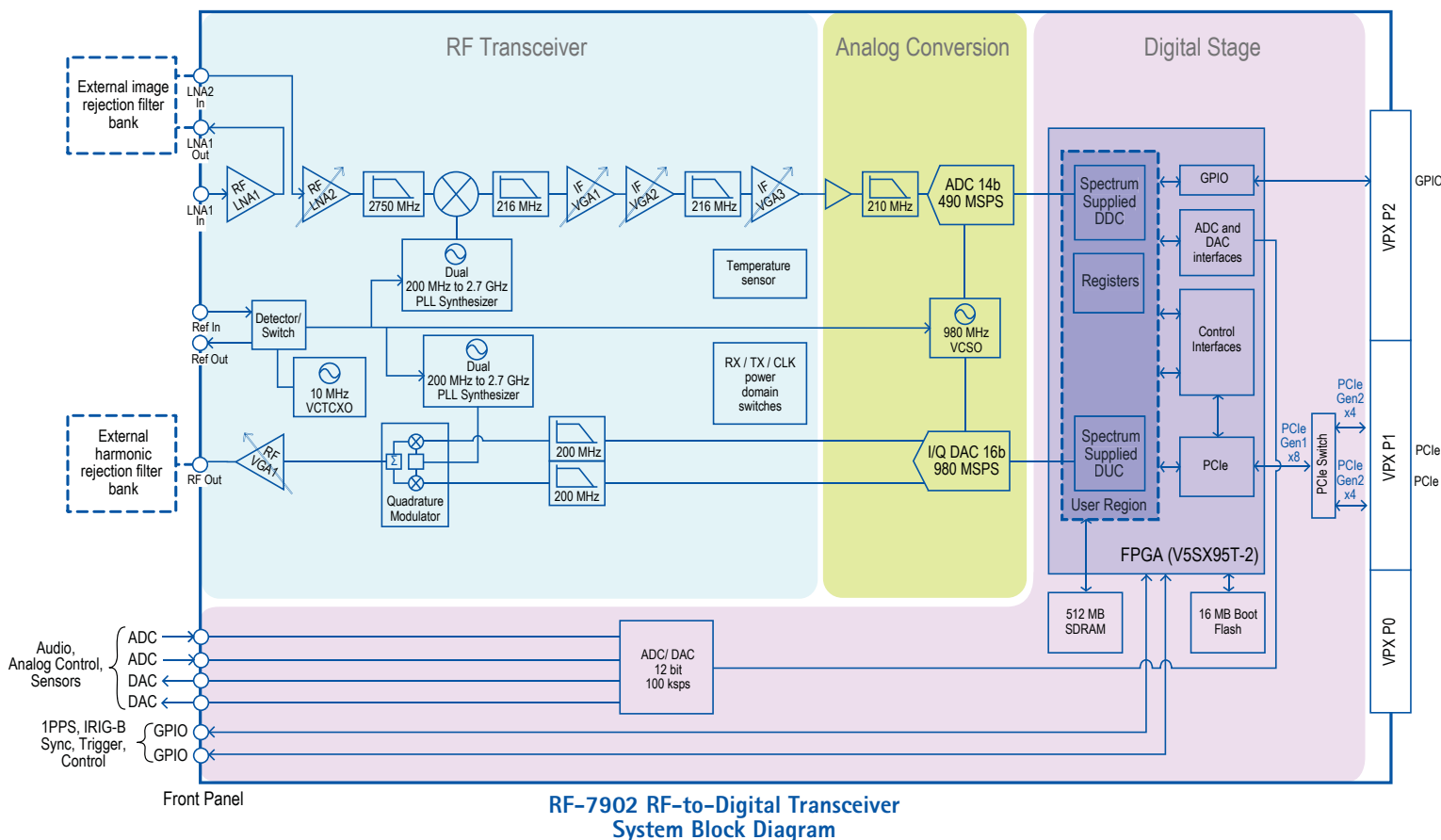




Fig. 1. Local Oscillator phase noise at 1 GHz (typical).

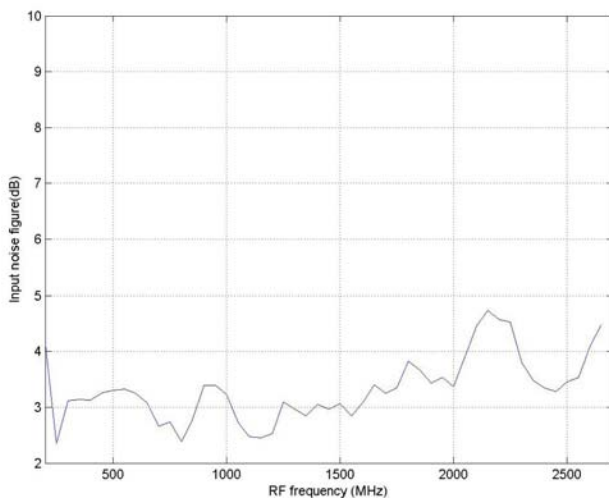


Fig. 2. Noise figure versus RF frequency using a QAM 16 signal (typical).

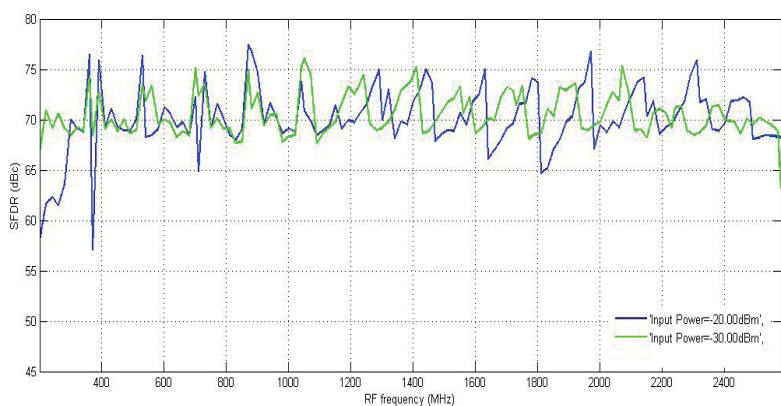


Fig. 2. SFDR versus RF frequency, 170 MHz bandwidth, input power -20 dBm and -30 dBm (typical).

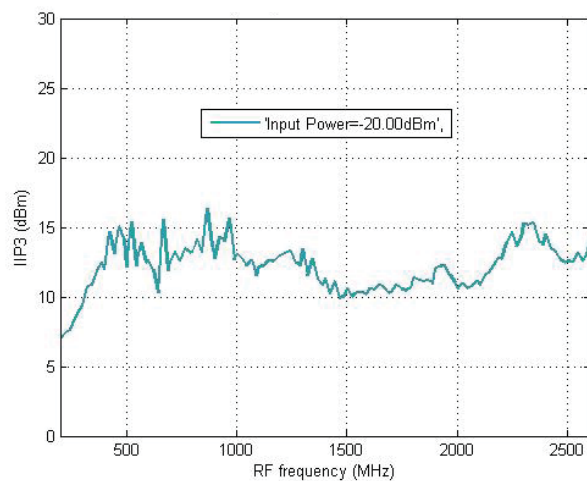


Fig. 3. IIP3 versus RF frequency, input power -20 dBm (typical).

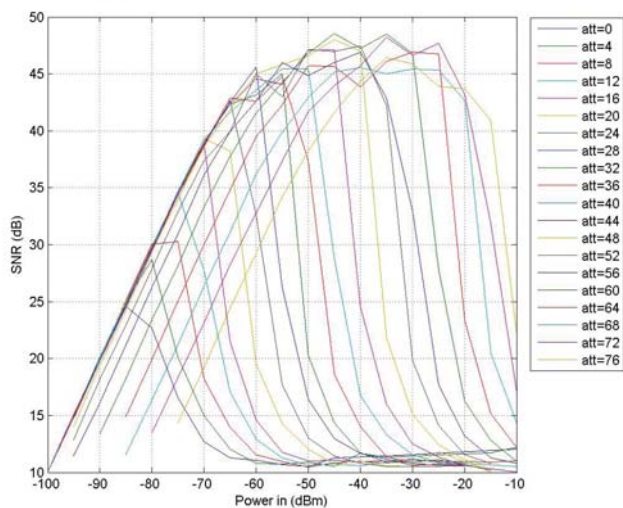


Fig. 4. SNR versus Input Power with 850 MHz RF input frequency attenuator step 4 dB over 0 to 76 dB LO (typical). SNR measured using a QAM 16 signal at 546,875 symbols per second using EVM.

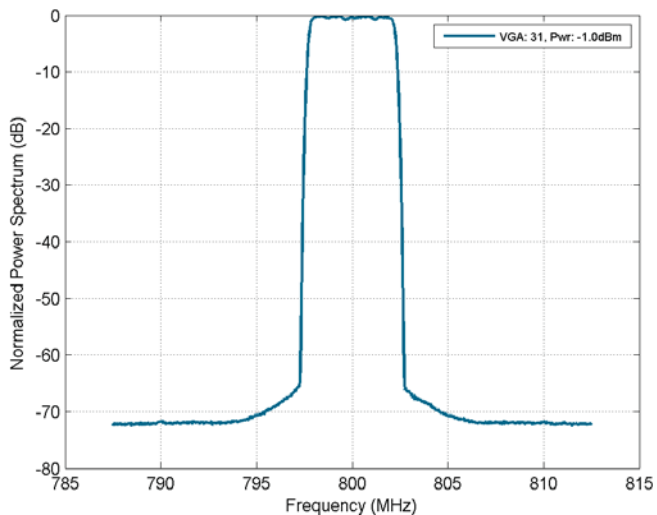


Fig. 6. Adjacent Channel Leakage Ratio (ACLR) at 800 MHz, 5 MHz bandwidth NPR signal, output power -1 dBm, 12dB PAPR backoff in DAC (typical)

Specifications

[general]	RF-to-Digital Transceiver Form Factor	Single channel full-duplex RF transceiver with Xilinx Virtex-5 FPGA 3U OpenVPX (VITA 65) Module Compatible with Module Profiles MOD3-PAY-1D-16.2.6-1, MOD3-PAY-1D-16.2.6-2, MOD3-PAY-2F-16.2.7-1, and MOD3-PAY-2F-16.2.7-2. For other module profiles, please contact Spectrum.
[RF - Receiver]	Receiver Type	Digitizing single-conversion superheterodyne
	Input Frequency Range	200 MHz to 2.7 GHz
	Internal Analog IF Frequency	User programmable from 20 MHz to 190 MHz
	Internal Analog IF Filtering	170 MHz LPF (BPF and other options, contact Spectrum)
	Analog Bandwidth	170 MHz standard, narrower bandwidth available
	Frequency Switching Time	20 μ s (dual switching synthesizer)
	Maximum Hop Rate	3,000 hops/sec with 10:1 dwell-to-tune time ratio
	Analog Frequency Step	400 kHz, smaller step sizes achieved digitally
	Maximum RF Input Power Level	-10 dBm
	IIP3	+10 dBm between 300 to 2700 MHz, +5 dBm between 200 to 300 MHz, two tone -20 dBm input power, gain adjusted for -1dBFS
	Gain Adjustment	78.75 dB adjustment range in 0.5 dB steps
	Noise Figure	2.8 dB at full gain at 800 MHz RF with image rejection filter
	LO SSB Phase Noise @ 1 GHz	-86 dBc/Hz @ 100 Hz offset -90 dBc/Hz @ 1 KHz offset -93 dBc/Hz @ 10 KHz offset -107 dBc/Hz @ 100 kHz offset
	Internal Reference Oscillator	10 MHz, +/- 2.0 ppm @ room temp
	Spurious Free Dynamic Range (SFDR)	75 dBc (typical) @ 1 GHz RF, 70 MHz IF, 10 MHz BW, input power -20 dBm 68 dBc (typical) @ full RF range, 170 MHz BW, input power -30 dBm
	Internal A/D Conversion	Intersil ISLA214P50 14 bit at 490 MSPS
	Image Rejection	User-supplied external filter. Contact Spectrum for custom filtering.
[RF - Transmitter]	Transmitter Type	Direct Up-Conversion
	Output Frequency Range	200 MHz to 2.7 GHz
	Output Power	-31 dBm to -3.7 dBm @ 10 dB PAPR, +6.3 dBm CW in 0.5 dB steps
	OIP3	+30 dBm at 1950 MHz to +32 dBm at 300 MHz at full power
	P1 dB	+22 dBm at 800 MHz
	Noise Floor	-140 dBm/Hz measured at 805 MHz in presence of a full power output CW signal at 850 MHz
	Adjacent Channel Leakage Ratio	-65 dBc at full output power, 850 MHz, 5 MHz bandwidth NPR signal
	Non-Harmonic Output Spurious	-60 dBc at 1.4 GHz at maximum power level
	Internal D/A Conversion	Analog Devices AD9122 16 bit interpolating DAC at 980 MSPS
	Internal Baseband Interface	Zero IF (I/Q) or Complex IF.
	Frequency Switching Time	20 μ s (dual switching synthesizer)
	Maximum Hop Rate	3,000 hops/sec with 10:1 dwell-to-tune time ratio
	Analog Frequency Step	400 kHz, smaller step sizes achieved digitally
	Harmonic Rejection	User-supplied external filter. Contact Spectrum for custom filtering.
[IF Processing]	User FPGA	Virtex-5 SX95T-2 (optional V5LX155T or SX50T). SX95T-2 has 94,208 logic cells, 640 DSP48E slices, and 8,784 kb total BRAM.
	FPGA IP	DDC and DUC included (user programmable IF bandwidth, IF frequency, and decimation)
	Memory	512 MB DDR2 SDRAM.
[external interfaces]	Control	PCIe from host SBC
	Analog Connectors	6 SMA, 50-ohm, single-ended (see block diagram)
	Analog GPIO	2x 12b 100 kSPS DAC, 2x 12b 100 kSPS ADC. Software support as a future option.
	Trigger/Interrupt Interface	PCIe
	High-Speed Serial Interfaces	One PCIe Gen1 x8 from FPGA to PCIe switch (2 GB/s full duplex) Two PCIe Gen2 x4 from PCIe switch to AMC backplane (2 GB/s full-duplex per port) 2 bi-directional high-speed serial lanes (can be configured for SRIO or Aurora*)
	FPGA Programming	Programming via JTAG or load from onboard 16 MB Flash
	FPGA Debug	Debug via JTAG with Xilinx JTAG device
	Digital GPIO	8x LVDS pairs, 11x 3.3V LVTTTL (5 are 5V tolerant), all via VPX P1/P2 connectors
	Co-Ax GPIO	Two co-ax single-ended available through the front panel (3.3V, 5V tolerant) (1PPS, IRIG-B, sync, trigger, control)
[electrical/mechanical]	Supply Voltage (DC)	5V, +12V
	Power Estimate	27 W booted. 30 W for full duplex operation. (~8 W for RF analog, ~22 W for digital)
	Size	3U OpenVPX form factor

[environmental]	Temperature	0 to +55 degrees C (air-cooled) -40 to +70 degrees C (conduction-cooled)
	Shock and Vibration	Conduction-cooled version: ANSI/VITA 47, Level ECC3 Conformal coating available on request.
	RoHS	5 of 6 compliant (Pb solder exemption).
	MTBF	Estimated at >300,000 hours (GB, GC, 30 deg C), per MIL-HDBK-217 FN2 Parts Count Method, Relx v8.0
[software]	Application Libraries Operating System	quicComm™ Software Development Kit with APIs and examples running on Host SBC Green Hills INTEGRITY 11 Fedora Linux 14
	Digital Up/Down Converter	FPGA-based DDC and DUC reference design provided featuring polyphase filter with variable bandwidth. User can control IF bandwidth, IF frequency and decimation with software to achieve frequency steps as small as 117 Hz.
[host SBC]		<ul style="list-style-type: none"> • Freescale QorIQ P3041 CES Creative Electronic Systems RIOV-2473 running Green Hills INTEGRITY 11, with RTM-6240 rear transition module. For more information, visit www.ces.ch. • Intel i7 Emerson Network Power IVPX7225 running Fedora Linux 14, with IVPX7225-RTM-1 rear transition module. For more information, visit www.emersonnetworkpower.com. • For other SBCs, please contact Spectrum.
[ordering information]	650-00632	RF-7902-CAC-SX95T-2 200-2700MHz Fast Tuning RF-Digital Transceiver 3U OpenVPX
[*future options]	User FPGA	Contact Spectrum Sales for options listed in this section.** V5LX155T or SX50T
	Analog GPIO	Software support for low speed ADC and DAC, e.g., Audio, Analog Control/Sensors
	Internal Analog IF Filtering	70 MHz BPF, 140 MHz BPF, or custom filtering, contact Spectrum
	High-Speed Serial Interface	Configure 2 bi-directional high-speed serial lanes for SRIO or Aurora
	Multi-board	Coherent operation across multiple RF-7902 modules
	RF Filtering	Contact Spectrum for external filter options
	Self Diagnostics	Built-In-Test (BIT)
	SCA BSP	Software Communications Architecture Board Support Package
	Object Request Broker	CORBA ORB
	Host	Contact Spectrum to discuss alternative host SBCs
	Operating System	Wind River VxWorks

Notes:

- Where applicable, RF specifications use a 10 MHz BW, Noise Power Ratio test signal. Contact Spectrum for other plots and specifications.
- Individual specifications on this datasheet are subject to change without notice. Do not specify compliance with this document.