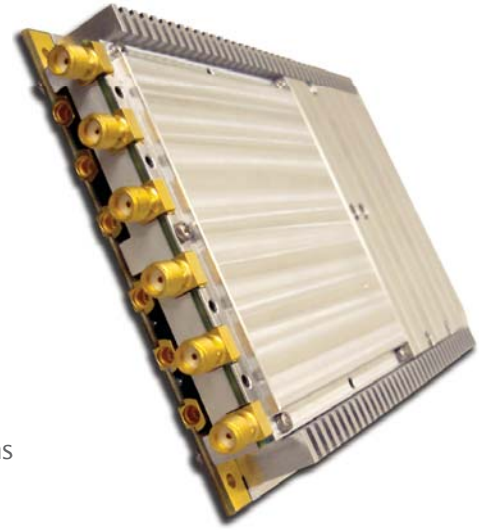
High Linearity Wideband RF-to-Digital Transceiver

RF-4902

3U cPCI

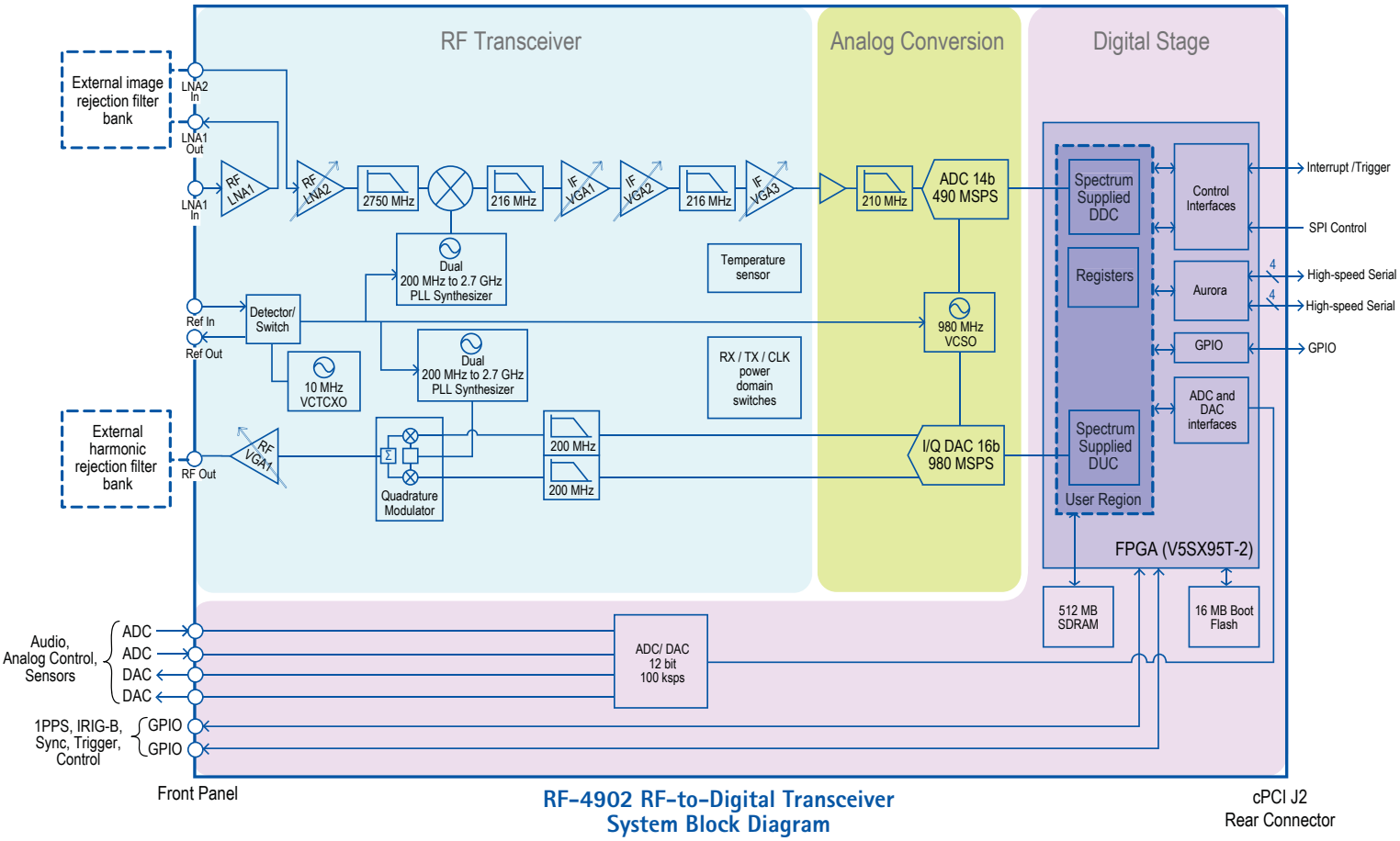
Features



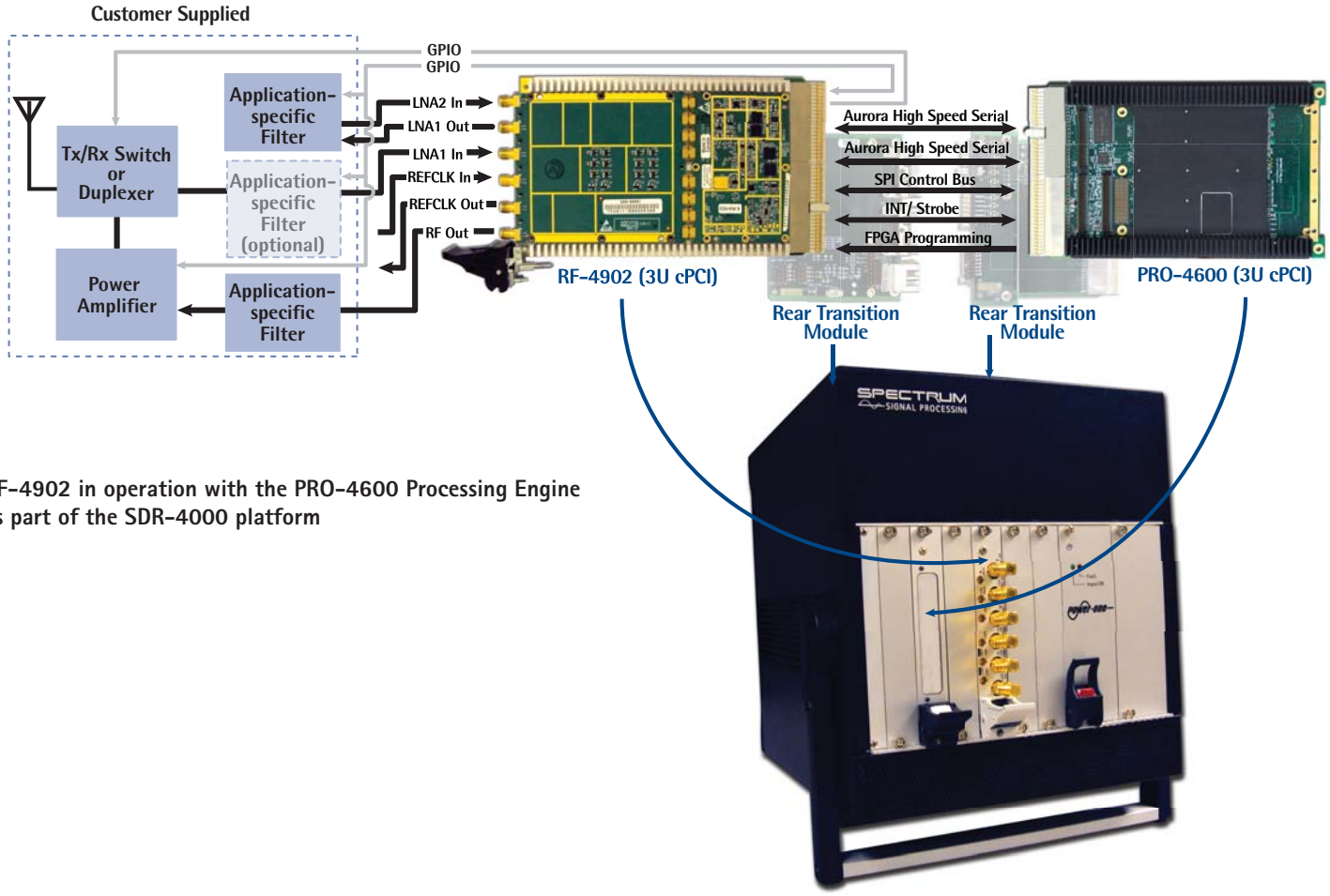
- Integrated RF and Digital IF Processing in a single 3U cPCI slot
- High linearity, wideband RF Transceiver, 200 MHz to 2.7 GHz
- 14-bit ADC 490 MSPS, 16-bit DAC 980 MSPS
- Fast-frequency hopping up to 3000 hops/sec
- Up to 170 MHz Receiver analog bandwidth
- Up to 400 MHz Transmitter analog bandwidth
- Xilinx Virtex-5 SX95T-2 User FPGA for flexible IF signal processing
- High-speed serial connection to companion baseband processor
- Software drivers and API, FPGA interface libraries, and example code included
- Digital Down Converter (DDC) and Digital Up Converter (DUC) IP included
- Rugged conduction- or air-cooled form factors available
- Designed to operate with Spectrum's PRO-4600 baseband processing engine as part of the SDR-4000 platform
- Not subject to US ITAR control

Applications

- Wideband Datalinks (eg. UAV, UGV, USV)
- Ground Mobile Communications
- Air-to-Ground Communications
- Communications Electronic Warfare
- SIGINT – COMINT/ELINT
- Satellite Ground Terminals
- Cognitive Radio
- Software Defined Radio (SDR) and Waveform Development



RF-4902 RF-to-Digital Transceiver System Block Diagram



RF-4902 in operation with the PRO-4600 Processing Engine as part of the SDR-4000 platform

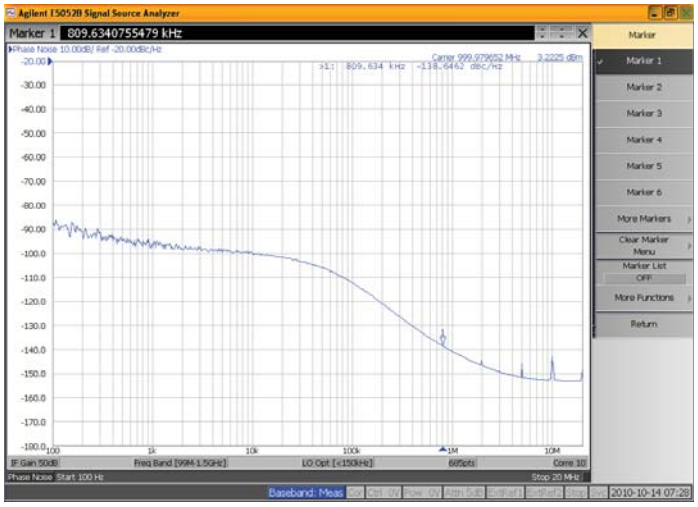


Fig. 1. Local Oscillator phase noise at 1 GHz (typical).

Fig. 2. Noise figure and gain versus frequency for first LNA (typical).

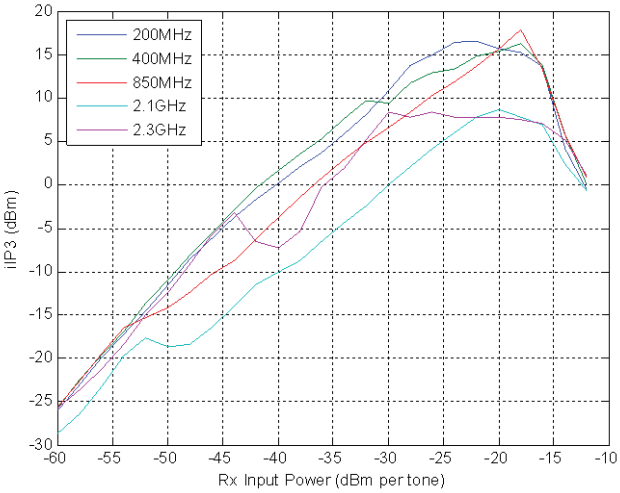


Fig. 3. Two-tone IIP3 versus RF input power (ADC input at -12 dBm per tone, held constant using VGA) (typical).

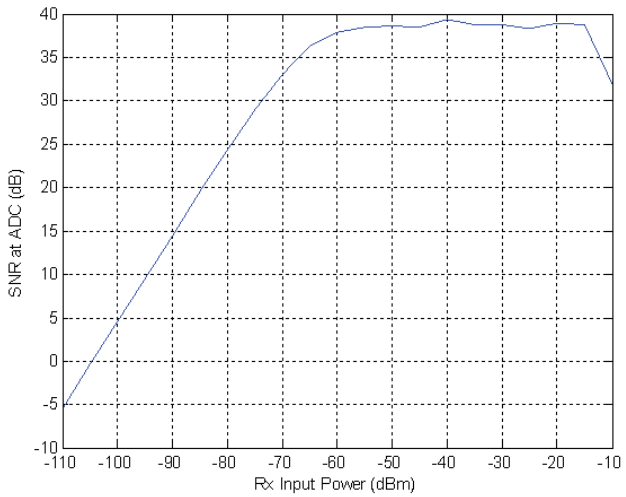


Fig. 4. SNR at ADC input versus Input Power (at 850 MHz 16 QAM-RRC 5 MSym/sec) (typical). Variable gain was reduced after input power reached -70 dBm.

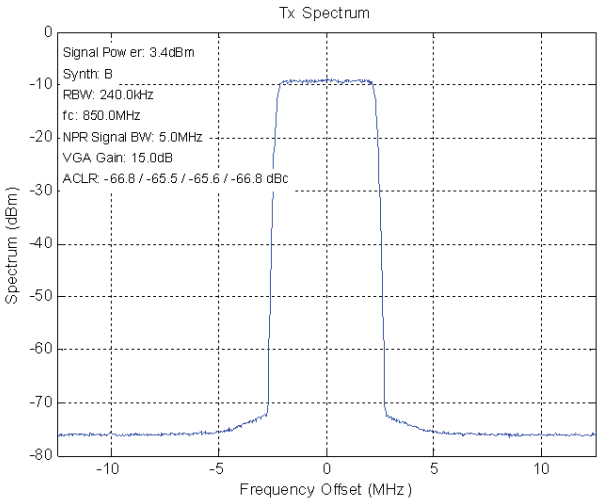


Fig. 5. Adjacent Channel Leakage Ratio (ACLR) at 850 MHz at full output power (typical).

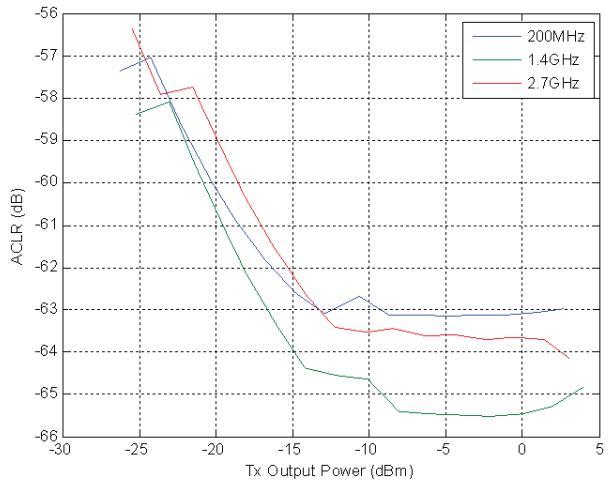


Fig. 6. Adjacent Channel Leakage Ratio (ACLR) vs. output power (typical).

Specifications

[general]	RF-to-Digital Transceiver	Single channel full-duplex RF transceiver with Xilinx Virtex-5 FPGA
[RF - Receiver]	Receiver Type	Digitizing single-conversion superheterodyne
	Input Frequency Range	200 MHz to 2.7 GHz
	Internal Analog IF Frequency	User programmable from 20 MHz to 190 MHz
	Internal Analog IF Filtering	170 MHz LPF (BPF and other options, contact Spectrum)
	Analog Bandwidth	170 MHz standard, narrower bandwidth available
	Processed IF Bandwidth	User programmable, measured at 10 MHz
	Frequency Switching Time	20 µs (dual switching synthesizer)
	Maximum Hop Rate	3,000 hops/sec with 10:1 dwell-to-tune time ratio
	Analog Frequency Step	400 kHz, smaller step sizes achieved digitally
	Maximum RF Input Power Level	-10 dBm
	IIP3	+5 dBm at minimum gain
	Gain	75 dB adjustment range in 0.5 dB steps
	Noise Figure	2.8 dB at full gain at 800 MHz RF with image rejection filter
	LO SSB Phase Noise @ 1 GHz	-86 dBc/Hz @ 100 Hz offset -90 dBc/Hz @ 1 KHz offset -93 dBc/Hz @ 10 KHz offset -107 dBc/Hz @ 100 kHz offset
	Internal Reference Oscillator	10 MHz, +/- 2.0 ppm @ room temp
	Spurious Free Dynamic Range (SFDR)	75 dB (typical @ 1 GHz,10 MHz BW)
	Internal A/D Conversion	Intersil ISLA214P50 14 bit at 490 MSPS
	Image Rejection	User-supplied external filter. Contact Spectrum for custom filtering.

[RF - Transmitter]	Type	Direct Up-Conversion
	Output Frequency Range	200 MHz to 2.7 GHz
	Output Power	-30 dBm to -3 dBm @ 10 dB PAPR, +7 dBm CW, in 0.5 dB steps
	OIP3	+30 dBm at 1950 MHz to +42 dBm at 200 MHz
	P1 dB	+22 dBm at 800 MHz
	Noise Floor	-140 dBm/Hz at full output power at 850 MHz
	Adjacent Channel Leakage Ratio	-65 dBc at full output power, 850 MHz, 5 MHz bandwidth NPR signal
	Non-Harmonic Output Spurious	-60 dBc at 1.4 GHz
	Internal D/A Conversion	Analog Devices AD9122 16 bit interpolating DAC at 980 MSPS
	Internal Baseband Interface	Zero IF (I/Q) or Complex IF.
	Frequency Switching Time	20 µs (dual switching synthesizer)
	Maximum Hop Rate	3,000 hops/sec with 10:1 dwell-to-tune time ratio
	Analog Frequency Step	400 kHz, smaller step sizes achieved digitally
	Harmonic Rejection	User-supplied external filter. Contact Spectrum for custom filtering.
[IF Processing]	User FPGA	Virtex-5 SX95T-2 (optional V5LX155T or SX50T). SX95T-2 has 94,208 logic cells, 640 DSP48E slices, and 8,784 kb total BRAM.
	FPGA IP	DDC and DUC included (user programmable IF bandwidth, IF frequency, and decimation)
	Memory	512 MB DDR2 SDRAM
[external interfaces]	Control	4-bit 10 MHz serial port interface (SPI) for control via cPCI J2
	Analog Connectors	6 SMA, 50-ohm, single-ended (see block diagram)
	Analog GPIO	2x 12b 100 kSPS DAC, 2x 12b 100 kSPS ADC. Software support as a future option.
	Trigger/Interrupt Interface	via ribbon cable on cPCI J2 using transition module
	High-Speed Serial	Two Aurora links (440 MB/sec full-duplex each) to the CompactPCI backplane via J2.
	FPGA Programming	Programming via JTAG over RTM from PRO-4600, or load from onboard 16 MB Flash
	FPGA Debug	Debug via JTAG with Xilinx JTAG device
	Digital GPIO	8x LVDS pairs, 18x 3.3V LVTTL, 3x 2.5V LVCMOS all via cPCI J2 connector
	Co-Ax GPIO	Two co-ax single-ended available through the front panel (3.3V) (1PPS, IRIG-B, sync, trigger, control)
[electrical/mechanical]	Supply Voltage (DC)	5V, 3.3V, -12V drawn from the CompactPCI J1 connector
	Power Estimate	27 W booted. 30 W for full duplex operation. (~8 W for RF analog, ~22 W for digital). 48 W combined operation with PRO-4600
	Size	3U CompactPCI form factor
[environmental]	Temperature	0 to +55 degrees C (air-cooled) -40 to +70 degrees C (conduction-cooled)
	Shock and Vibration	Conduction-cooled version: ANSI/VITA 47, Level ECC3 Conformal coating available on request.
	RoHS	5 of 6 compliant (Pb solder exemption).
	MTBF	370,000 hours (GB, GC, 30 deg C), per MIL-HDBK-217 FN2 Parts Count method, Relex v8.0.
[software]	Application Libraries	*quic*Comm™ Software Development Kit with APIs and examples running on PRO-4600
	Operating System	Green Hills INTEGRITY 5.0.11 or Wind River VxWorks 5.5
	SCA BSP	Software Configuration Architecture Board Support Package for SDR-4902 systems available (for INTEGRITY OS only). Contact Spectrum Sales.
	Digital Up/Down Converter	FPGA-based DDC and DUC reference design provided featuring polyphase filter with variable bandwidth. User can control IF bandwidth, IF frequency, and decimation with software to achieve RF frequency steps as small as 12.5 kHz.
[ordering information]	650-05010	RF-4902-CAC-SX95T-2 200-2700MHz Fast Tuning RF-Digital IF Up/Down Converter 3UcPCI
[*future options]		Contact Spectrum Sales for options listed in this section.**
	User FPGA	V5LX155T or SX50T
	Analog GPIO	Software support for low speed ADC and DAC, e.g., Audio, Analog Control/Sensors
	Internal Analog IF Filtering	70 MHz BPF, 140 MHz BPF, or custom filtering, contact Spectrum
	Multi-board	Coherent operation across multiple RF-4902 modules
	Host	Contact Spectrum for alternative hosts other than PRO-4600
	Form Factor	OpenVPX
	RF Filtering	Contact Spectrum for external filter options
	Self Diagnostics	Built-In-Test (BIT)
	Operating System	Linux (for VPX form factor)

Notes:

- Where applicable, RF specifications use a 10 MHz BW, Noise Power Ratio test signal. Contact us for other plots and specifications.
- Individual specifications on this datasheet are subject to change without notice. Do not specify compliance with this document.

SPECTRUM SIGNAL PROCESSING by Vecima

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