Advanced FPGA Verification with Questa Seminar

Agenda

- 09:00 – 09:30 Registration
- 09:30 – 09:40 Welcome and Introduction
- 09:40 – 09:55 Why you need a Verification Process
- 09:55 – 10:10 Three Steps to injecting Automation
- 10:10 – 10:20 Break
- 10:20 – 10:50 Reduce debug Time by 50%
- 10:50 – 11:20 Understand where you are in the Verification Process
- 11:20 – 12:00 Build an effective Testbench Infrastructure
- 12:00 – 13:00 Lunch
- 13:00 – 13:45 The Vivado Design Flows
- 13:45 – 14:45 Vivado Visualization capabilities
- 14:45 – 15:15 Xilinx design constraints (XDC) introduction
- 15:15 – 16:00 Summary, Closing Remarks, Draw

Jun 11, 2013 Register

Waterloo, Ontario

8:30 AM - 4:00 PM US/Eastern

Jun 13, 2013 Register

Ottawa, Ontario

8:30 AM - 4:00 PM US/Eastern