VESA Display Stream Compression (DSC) Primer

HDT-DSC100 (v1.0H)

Course Specification

Course Description

This one-day course provides a foundation for the newly-adopted VESA DSC v1.1 video compression technology. The course begins with an introduction to the basics of the underlying structure of DSC video algorithms and evolves to explore DSC applications, usage models, system architecture and implementation challenges for DSC encoder and decoder designs. The course concludes with an overview of the resources available at VESA, as well as considerations and practical recommendations on how to design a product compatible with the VESA DSC v1.1 video compression standard.

Price – $800 USD
Course Duration – 1 day
Course Part Number – HDT-DSC100-ILT
Who Should Attend? – System architects, engineers and designers who have an interest in using DSC for mobiles, tablets, TV and other display applications.
Prerequisites

- None

Course Outline

DSC introduction - introduces basic concepts and origins of DSC. What are the system benefits and economical considerations. Market segments addressed.

VESA DSC 1.1 Standard

- DSC fundamentals: Understanding DSC compression, slices encoding and decoding. Rate control, rate buffer.
- DSC algorithms: Prediction modes, prediction loops, indexed color history, encoding decision process, VLC encoding, sub-stream multiplexing and slice multiplexing.

Applications, usage models and system architecture

- Architecture overview
- MIPI DSI 1.2 applications: video and command modes
- Embedded DisplayPort 1.4 applications

Encoder implementation challenges

- Product requirements and performance objectives
- Encoder architecture elements: data flow and pipelining. Context switch. Algorithm sub blocks implementation. Rate Controller, sub stream multiplexing. Slice multiplexing and rate buffer sizing.

Decoder implementation challenges

- Product requirements and performance objectives
- Encoder architecture elements: data flow and pipelining. Context switch. Algorithm sub blocks implementation. Rate Controller, sub stream multiplexing. Slice multiplexing and rate buffer sizing.

DSC design: how to get started?

- VESA information available: C-model and standard specifications
- Compliance Test Guide (CTG)
- Interoperability considerations

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Email: training@hardent.com
Telephone: 514-284-5252