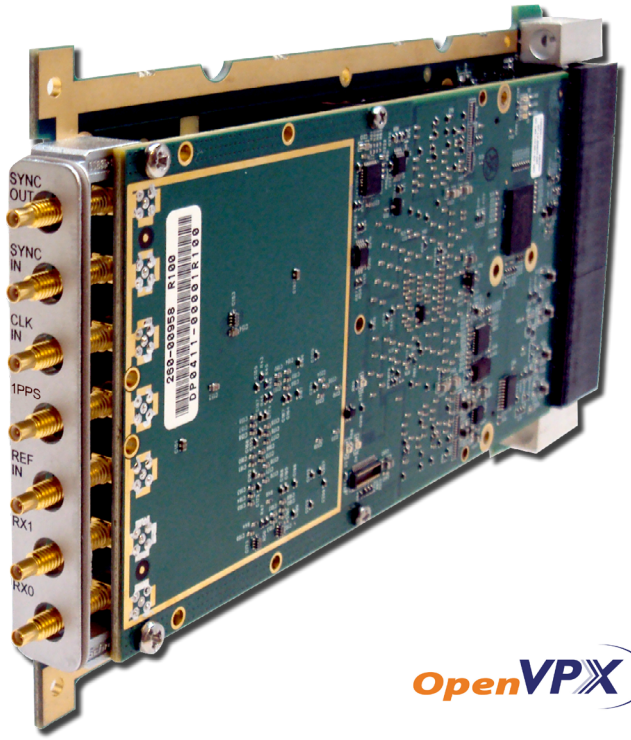
Wideband Digital Receiver/Digitizer Module
VPX-1151

VPX

Product Overview

The VPX-1151 is an ultra high-speed digitizer and processing solution that enables direct RF-to-Digital conversion between 2 MHz and 3 GHz.

It complies with OpenVPX (VITA 65), the architecture framework that defines system-level VPX interoperability for multivendor, multimodule systems.



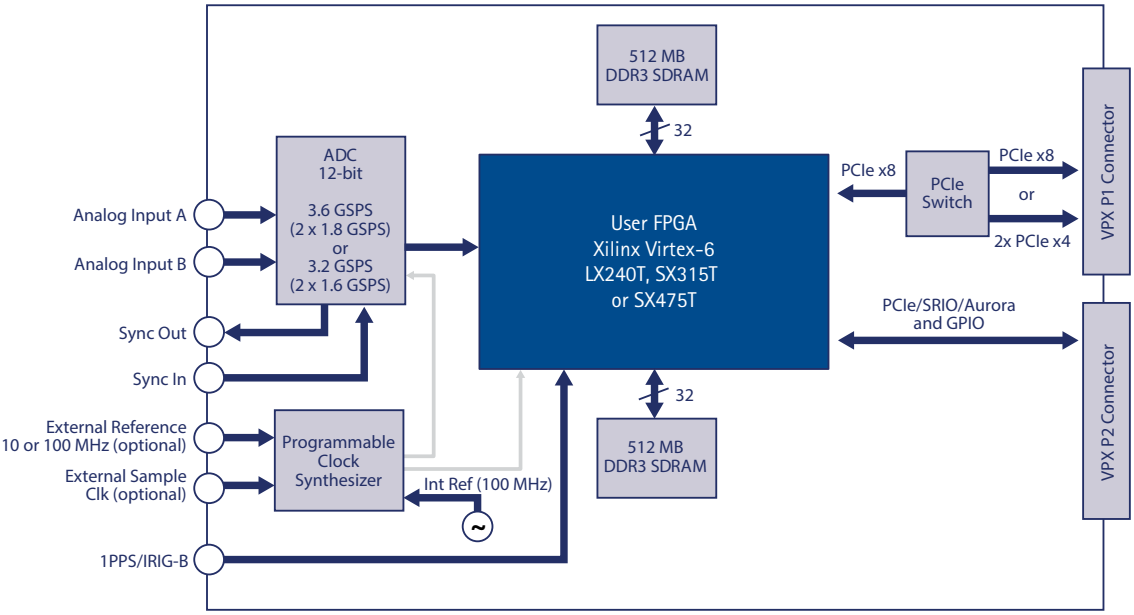
OpenVPX™

Features

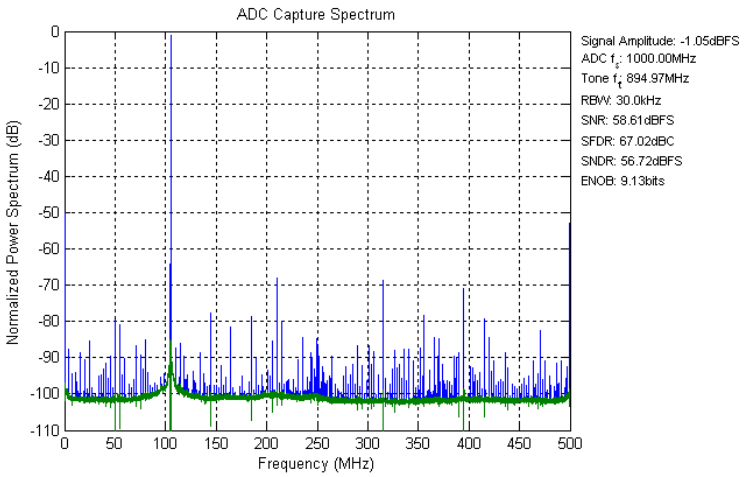
- One 3.6 GSPS 12-bit ADC channel (or two channels at 1.8 GSPS); or One 3.2 GSPS 12-bit ADC channel (or two channels at 1.6 GSPS)
- ADC analog input bandwidth up to 2.8 GHz enables bandpass sampling (2nd, 3rd, or 4th Nyquist zone)
- Supports multi-board synchronization
- Support for phase coherent sampling
- Xilinx Virtex-6 SX315T or LX240T User FPGA
- 1 GB DDR3 SDRAM (2 banks of 512 MB, 1066 Mbps)
- PCI Express x8 Gen 2 (VITA 42.3) (4 GB/s full-duplex)
- General purpose digital I/O including high speed serial
- Drivers and Linux SDK, API, FPGA interfaces included
- Digital downconverter (DDC) IP available
- Air-cooled, rugged conduction-cooled available

Applications

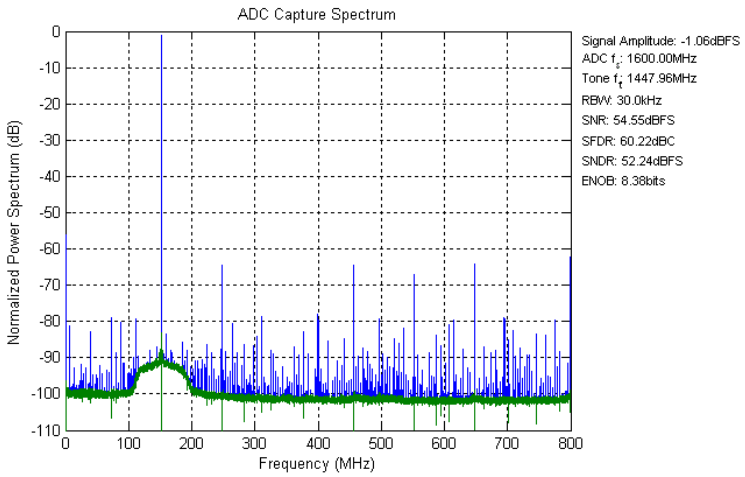
- SIGINT (COMINT/ELINT)
- RADAR
- Satellite Receiver
- Electronic Support Measures (ESM)
- Spectral Analysis
- Wideband Signal Recorder
- Software Defined Radio (SDR)
- High-Speed Test and Measurement
- Set-Top Box Development
- Wideband Sensing for Cognitive Radio
- Channel Measurement and Characterization



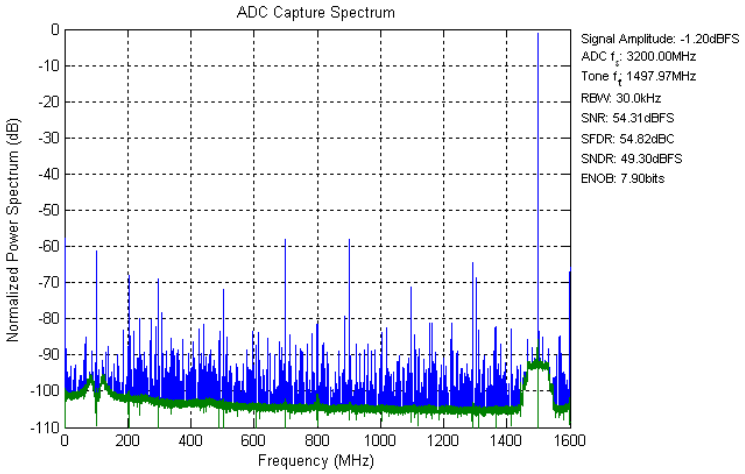
VPX-1151 Block Diagram



Sample spectral plot for 895 MHz input signal at 1.0 GSPS



Sample spectral plot for 1448 MHz input signal at 1.6 GSPS



Sample spectral plot for 1498 MHz input signal at 3.2 GSPS

Spectrum Signal Processing by Vecima tel +1/604.676.6700 or +1/800.663.8986 fax +1/604.421.1764 www.spectrumsignal.com

Specifications

[general]	Form Factor	3U OpenVPX (VITA 65) Module Compatible with Slot Profiles MOD3-PAY-1D-16.2.6-1, MOD3-PAY-1D-16.2.6-2, MOD3-PAY-2F-16.2.7-1, and MOD3-PAY-2F-16.2.7-2
	User Programmable FPGA	Xilinx Virtex-6 SX315T-2, LX240T-2 or SX475T
	Memory	1GB DDR3 SDRAM (2 banks of 512 MB each, 1066 Mbps)
	Sample Clock	Internal clock synthesizer 900-1600 MHz (900-1800 MHz for 12D1800 ADC)
	Reference Clock	Internal 10 MHz clock reference (+/- 2.0 ppm) or external reference input 10 or 100 MHz
[analog I/O]	A/D Converter	Texas Instruments ADC12D1600 12-bit (up to 3.2 GSPS single channel/1.6 GSPS dual channel) or ADC12D1800 12-bit (3.6 GSPS single channel/1.8 GSPS dual channel)
	ADC Input	AC coupled, single-ended Full scale input: 0 dBm 50 ohms typical Analog full power bandwidth: 2 MHz to 2.8 GHz (AC coupled dual-channel mode)
	ADC Characterization (typical)	

895 MHz Fin with 1.0 GSPS	1448 MHz Fin with 1.6 GSPS	1498 MHz Fin with 3.2 GSPS
ADC SFDR = 62.0 dBc	ADC SFDR = 60.2 dBc	ADC SFDR = 54.8 dBc
ADC SNR = 58.6 dBFS	ADC SNR = 54.5 dBFS	ADC SNR = 54.3 dBFS
ADC ENOB = 9.1 Bits	ADC ENOB = 8.4 Bits	ADC ENOB = 7.9 Bits
ADC SFDR = 61 dBc	ADC SFDR = 62 dBc	

	Ext. Clock	
[external interfaces]	Analog Input	SSMC 50 ohms, 0 dBm typical
	External Reference Clock	SSMC 50 ohms, 0.75 - 1.6 Vpp 10 MHz clock reference
	External Sampling Clock	SSMC 50 ohms, -3 dBm typical 800-1600 MHz (800-1800 MHz for 12D1800 ADC)
	GPS Timing Reference	SSMC 50 ohms, 1PPS/IRIG-B TTL/LVTTL
	Sync Input/Output	Twinax 100 ohms differential connector (auto-sync for multi-board phase coherency)
	VPX Interface	PCIe Gen 2: one x8 link or two x4 links, providing 4 GB/s (full-duplex) bandwidth to VPX P1 connector Configurable connection to VPX P2 connector: GPIO (1 pair LVDS clock with 16 pairs LVDS data and 4 single-ended LVTTL) plus PCIe Gen 2 x8 (can be configured for SRIO or Aurora*)
	JTAG Connection	JTAG connector for Virtex-6 FPGA, Xilinx Chipscope debugger compatible
[compatibility]	Supported Host OS	Red Hat Enterprise Linux 6.5 or Green Hills INTEGRITY 11
[development software]	Application Libraries	quicComm Software Development Kit with system-level example source code
	Multi-board Sync	Firmware to support phase coherent sampling
	FPGA Code Development	Support for ISE Foundation tools from Xilinx or Synplify-Pro from Synopsys, Simulink/System Generator, ModelSim PE from Mentor Graphics
	HDL Coding Language	VHDL
[electrical]	Supply Voltage (DC)	+3.3V, +5V and +12V VPWR
	Power estimate	25W (typical) - depends on FPGA size and usage
[environmental]	Operating Temperature	Air-cooled: range of 0 to 50 C, forced air at 600 LFM Industrial conduction cooled: -40 to 70 C card edge
	Shock and Vibration	Conduction cooled version VITA-47 level CC3 tested in accordance with MIL-STD-810F
	Humidity	5-95% non-condensing. Contact Spectrum for higher ranges. Conformal coating available.
	RoHS	5/6 compliant (Pb solder exemption)
	MTBF	692,000 hours (GB, GC, 30 deg C), per MIL-HDBK-217 FN2 Parts Count method, Relex v8.0.
[ordering information]	650-00624	VPX-1151-CAC-V6LX240T-2-1GB 12b 3.2 GSPS ADC
	650-00618	VPX-1151-CAC-V6LX240T-2-1GB 12b 3.6 GSPS ADC
	650-00639	VPX-1151-CAC-V6LX315T-2-1GB 12b 3.2 GSPS ADC
	650-00637	VPX-1151-CAC-V6LX315T-2-1GB 12b 3.6 GSPS ADC
	650-00640	VPX-1151-CAC-V6LX475-2-1GB 12b 3.2 GSPS ADC
	800-00537	VPX-1151-CAC-V6LX240T-2 3.2 GSPS Quickstart Kit for VPX 3U Air-Cooled (includes software, documentation, and cable kit)
	800-00533	VPX-1151-CAC-V6LX240T-2 3.6 GSPS Quickstart Kit for VPX 3U Air-Cooled (includes software, documentation, and cable kit)
	800-00549	VPX-1151-CAC-V6LX315T-2 3.2 GSPS Quickstart Kit for VPX 3U Air-Cooled (includes software, documentation, and cable kit)
[future options**]	A/D Conversion	12-bit at 2.0 GSPS single channel or dual channel at 1.0 GSPS 12-bit at 1.0 GSPS single channel or dual channel at 500 MSPS
	Memory	2 GB DDR3 SDRAM (2 x 1 GB banks)
	ADC input	DC coupled
	*SRIO/Aurora	Software and FPGA support
	Operating System	VxWorks, Windows

SPECTRUM SIGNAL PROCESSING
by Vecima

Rev 2014.06.27_TD.MB.CF

Spectrum Signal Processing by Vecima tel +1/604.676.6700 or +1/800.663.8986 fax +1/604.421.1764 www.spectrumsignal.com