

Dual Fixed and Floating Point C6670 Multicore DSP Processing Engine

VPX-8320

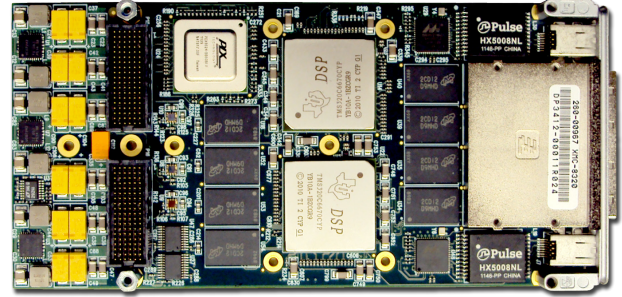
Product

Description

Powerful, high-performance fixed-point and floating-point DSP signal processing engine in an OpenVPX form factor (VITA 65).

Key Features

- Two TI quad-core TMS320C6670 DSPs
- Fixed and floating point up to 26.6 GMacs per core @ 1 GHz / 16 GFlops per core @ 1 GHz
- 1 GB of DDR3 SDRAM per DSP
- High-speed 40 Gbit TI Hyperlink interprocessor communications (between DSPs)
- VPX module supporting PCI Express x4 Gen 2 (VITA 42.3) (2 GB/s full-duplex)
- Front panel I/O: AIF (2 ports, 4 lanes each)* and GigE* (2 ports)
- VPX P2 High-speed serial I/O: SRIO* (6 lanes), AIF* (2 lanes) and SGMII* (2 lanes)
- VPX P2 Single-ended I/O: GPIO (14 pins), RS-232
- C6670 is binary backwards compatible with C67xx, C64x and C62x



Sample Applications

- Satellite Communications (SATCOM) including satellite earth stations
- LTE/WiMAX development and test
- Industrial Control
- Signals Intelligence (SIGINT-COMINT/ELINT)
- Software Defined Radio (SDR)
- Cellular base station development and test
- High density DSP processing

Features of the C6670 DSP

- Please refer to TI datasheets for full details: <http://www.ti.com/product/tms320c6670>
 - 4 cores
 - Wireless coprocessor (Integrated Viterbi, Turbo, and FFT)
 - Antenna interface for OBSAI/CPRI

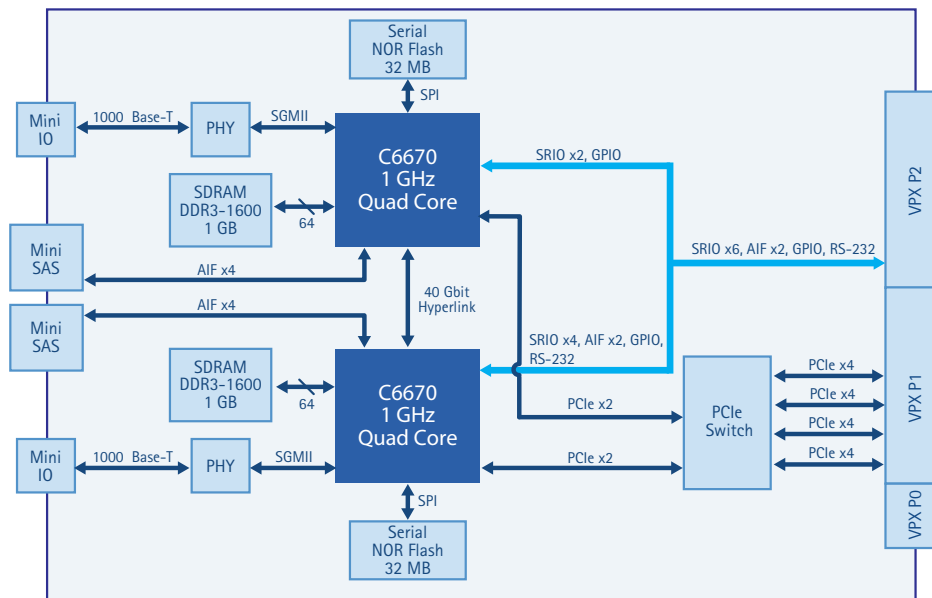


Figure 1. VPX-8320 block diagram

*see "Future Options" section

VPX

Specifications

[general]	Form Factor	3U OpenVPX (VITA 65) Module Compatible with Slot Profiles MOD3-PAY-1D-16.2.6-1, MOD3-PAY-1D-16.2.6-2, MOD3-PAY-2F-16.2.7-1, and MOD3-PAY-2F-16.2.7-2
	Processors	Two 1 GHz TMS320C6770 fixed-point and floating-point DSPs from Texas Instruments
	Memory	1 GB of DDR3 SDRAM per DSP
	DSP Clock Speed	1 GHz
[external interfaces]	PCIe	From each DSP to PCIe switch: PCIe x2 Gen 2 From PCIe switch to VPX P1 connector: 4 ports of PCIe x4 Gen 2 (2 GB/s full duplex) (VITA 42.3)
	I/O	VPX P2 serial: SRIO* (6 lanes), AIF* (2 lanes), RS-232 VPX P2 single-ended GPIO: 30 (8 dedicated pins from each DSP, plus 14 pins factory configurable to connect to DSPs or PCIe switch Front panel: AIF (2 ports Mini SAS connector, 4 lanes each) and GigE (2 ports Mini IO)
	JTAG Connection	Available for debug support via connector accessible on solder side of the board
[onboard fabric]	Between DSPs	High-speed 40 Gbit TI hyperlink interprocessor communications
[performance]		2 DSPs per XMC module, 4 cores per DSP For more details, please refer to the TI C6670 datasheet
	Fixed point	up to 26.6 GMacs per core @ 1 GHz
	Floating point	up to 16 GFlops per core @ 1 GHz
[host requirements]	Supported Host OS	RedHat Enterprise Linux 5.9 on INTEL i7 SBC GHS INTEGRITY 11.0.4 on CES RIOV-2473JE SBC
[development software]	quicComm	The quicComm software suite supports on both the host and target processors. quicComm provides functions for: <ul style="list-style-type: none"> • Configuration and control • Initiating PCIe DMA data transfers It also provides a complete set of examples
[other software]	Debug Support	Support for TI's Code Composer Studio via JTAG emulator is provided (JTAG emulator sold separately)
[electrical]	Supply Voltage (DC)	+3V and +5V
	Power Estimate	TBD
[mechanical]	Size	Standard VITA 46 VPX 3U (100mm(high) x 160mm(deep), 0.8 or 1.0 inch pitch)
[environmental]	Operating Temperature range	0 to 50° C forced air
	RoHS	5 of 6 compliant
[future options]	Operating Temperature range	-40 to 70° C forced air
	RoHS	6 of 6 compliant
	Interfaces	Software support for AIF, GigE, SRIO
	Hyperlink	Speed increase to 50 Gbps (when available on the C6670 DSP)

*see "Future Options" section

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