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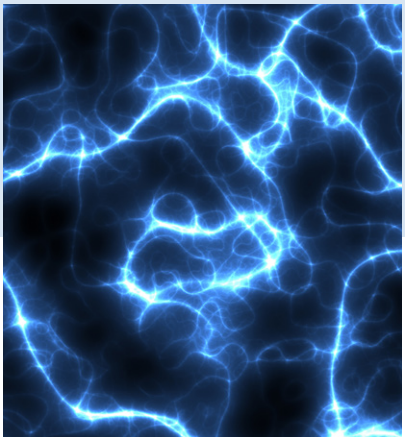

ESD concerns with PCB assembly: Barcode Labeling and Masking

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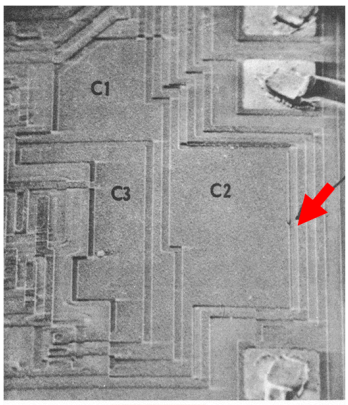
INTRODUCTION:

The manufacture or assembly of printed circuit boards (PCB) is a complex and challenging process. An on-going trend with PCB design is that they are becoming smaller, more complex, and dense with layers of circuitry and components. The challenge for a design engineer is to design a PCB that will meet intended use, but with a design that will operate flawlessly under adverse conditions and for the life of the device.

A challenge to meeting these objectives is to have the device or PCB survive and/or be tolerant to an electrostatic discharge (ESD). An ESD event can cause physical damage (e.g., surface oxidation, material loss) to circuits; either printed on the PCB or embedded in a component. ESD can also result in latent defects, resulting in reliability concerns. There are many components on PCBs that are vulnerable to ESD; they include microcircuits, discrete semiconductors, thick and thin film resistors and piezoelectric crystals. All need precautions to prevent damage from an ESD event.[1,11]

Figure 1: ESD damage; C2 MOS Microcircuit Damage[14]



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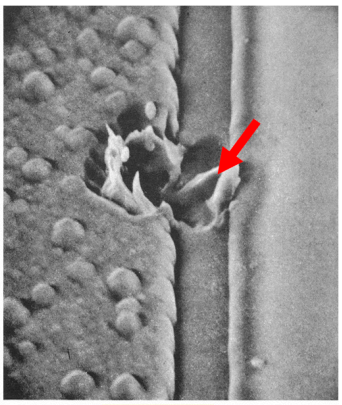

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THE ESD PROBLEM:

The ESD problem in electronics production and especially PCB assembly (PCBA) is significant. The ESD damage can be seen immediately during assembly when a circuit stops functioning or later on during the life of the device. This latent ESD failure adds to the "cost of ESD" with repair costs, return costs, and end-user disappointment. The industry has estimated that product losses due to ESD can be up to 7%.[3]

To understand the static problem, it is important to understand where static comes from. The main source of static comes when two dissimilar surfaces are brought into contact and then separated. The charge imbalance on each of the separated surfaces creates an electrical potential that may enable that charge to subsequently move. In PCBA, there are several key processes that create triboelectric charge; they include human contact, machine contact (conveyors, robotics, etc.), component mounting, applying solder paste, tape masking and barcode labeling. All sources require consideration when developing an ESD control program. [2,6,7]

Figure 2; PCBA process; M-Wave – China Work Centers [2]

The first step taken by a PCB designer is to determine the sensitivity of the PCB and components to electrostatic discharge. Often the designer will rely on data supplied by suppliers (i.e., component manufacturers) for ESD sensitivity levels. These manufacturers will characterize the sensitivity based on exposure to humans and machines. They will use models such as the human body model (HBM) and charged device model (CDM) to classify ESD sensitivity. In simple terms, the main difference between the two models is the rate of discharge with the human body releasing charges (slower) than when metal to metal contact occurs in the CDM events. However, even if humans and machines have the same 5kV potentials, the rate of discharge is slower for the human and components may react differently to the different discharge rates. [1,8,11]

As an example, a CMOS component may have a sensitivity of 1000V for the HBM, but only a 500v CDM. PCB and component manufacturers may use the ESD threshold classification to characterize their part. As an example, appendix 1 shows ESD sensitivity for a Texas Instruments Load Switch that has ESD sensitivity levels of 2kV and 1kV for HBM and CDM, respectively. The following table used in the ANSI/ESD S5.3.1 standard contains the HBM and CDM threshold classifications. [14,15]

Table 1: Device Thresholds as specified in ANSI/ESD S5.3.1

VOLTAGE RANGE	HBM CLASSIFICATIONS	CDM CLASSIFICATION
<125	—	C1
125 to <250	0	C2
250 to <500	1A	C3
500 to <1000	1B	C4
1000 to <1500	1C	C5
1500 to <2000	1C	C6
2000 to <4000	2	C7
4000 to <8000	3A	C7
>8000	3B	C7

If a PCB designer is using electronic components that are deemed HBM Class 0 or CDM Class C2 sensitive, a robust ESD control plan is needed. That plan would need to consider all aspects of PCB assembly and make sure that three key elements are defined and resolved. [9] They include:

a. All conductors need to be grounded. A charged isolated conductor can be a dangerous risk.

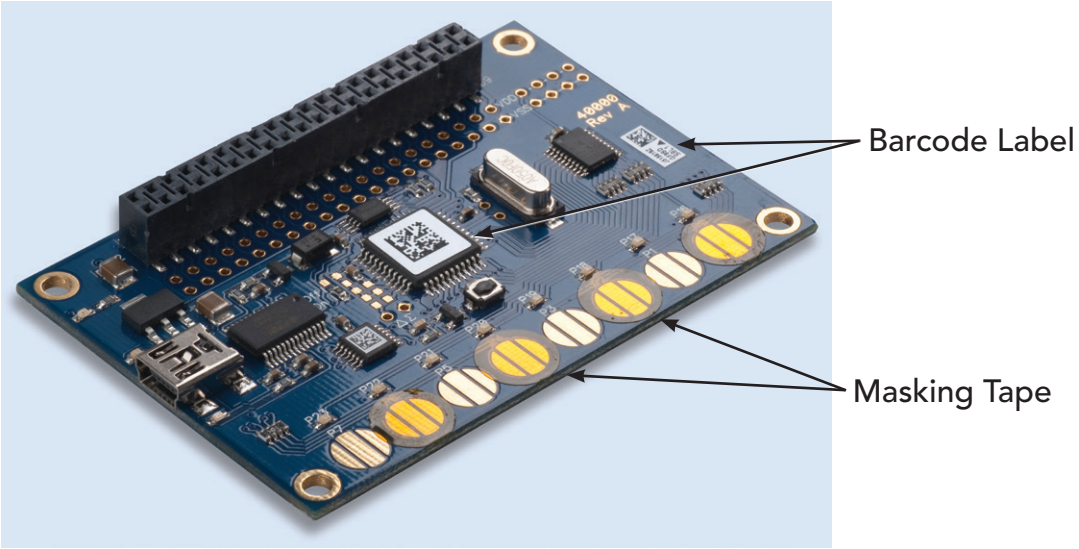
b. Non-conductors (insulators) need to be replaced with static dissipative/ low charging materials whenever possible.

c. Transportation of the device outside of ESD protected areas (EPA) requires static protective materials (static safe packaging).

ESD Source: Masking Tape and Barcode Labels [2,3,4,5,11]

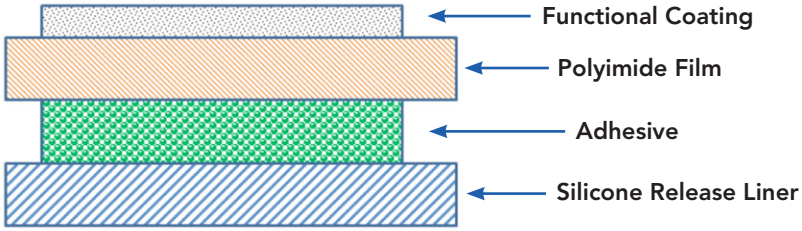
For this paper, we will consider in depth the role masking tape and barcode labels have in creating risk of an ESD event and steps that can be taken to reduce this risk. Both materials play an important role in PCBA. The masking tape provides protection to components during the assembly process by covering or masking sensitive components from flux, solder, and cleaning agents. The barcode label is important in providing a tracking means for PCB during the assembly process. Most robust manufacturing processes collect data on the PCB during each assembly step and allow for lot tracking via the barcode. Using a label printed on-demand at the site of manufacture offers a cost effective and flexible way to barcode the PCB.

Figure 3: PCB with label and masking tape



For PCBA, the label and tape are typically cut into small shapes and are constructed of a film and adhesive that is supported on a release liner. Since the PCB goes through a harsh set of conditions including high temperatures and harsh chemical exposure, the tapes and labels use a high temperature film like polyimide or polyester. Typically, the label will have a white coating that allows ink to adhere and provides contrast for scanning the barcode. Similarly the tape may have a functional coating on the surface of the polyimide film. The following is a typical cross section of a PCB masking tape and barcode label.

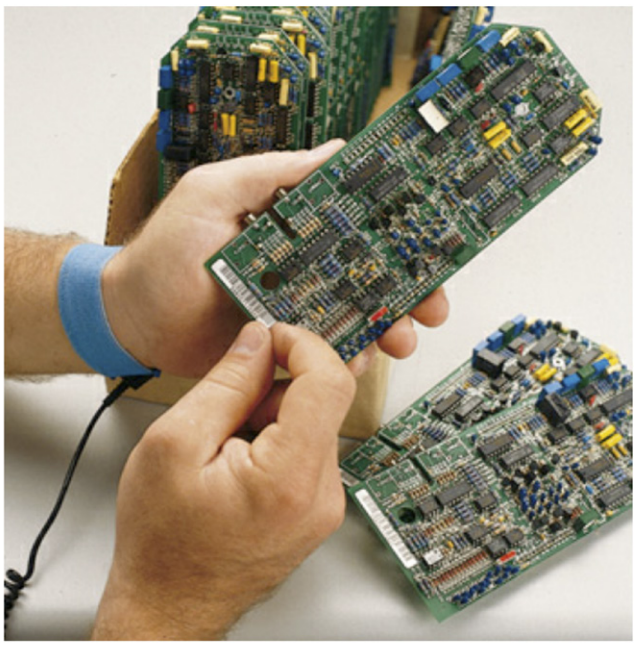
Figure 4: Barcode label and masking tape cross section.



Both the label and tape produce similar static discharge concern(s). Before being applied to the PCB, both the tape and label are removed from the release liner. This can be done manually or automatically with a machine. By its nature, the adhesive and liner are poorly bonded, which allows for easy release when separating. This poor bond is achieved by using a coating on the liner that is chemically dissimilar to the adhesive. The dissimilar chemistry causes a poor "wetting" of the adhesive that yields the poor bond. However, the dissimilar nature of the adhesive and liner causes a negative effect, in that they may produce a significant triboelectric charge when separated (or pulled apart). So, during the application process, the charged adhesive will induce a charge in conductive items (including circuitry). Measurements of charge potential of label and tapes removed from liner can be greater than 5kV, depending on size.

A complicating factor to this triboelectric charge on the adhesive during the application process is whether the label is applied by hand or by an application machine. Any charge introduced by the human or the applicator machine can add to the charge potential of the label or tape and increase the discharge risk. In addition to this apparent risk, because the label/tape is a charged insulator it can create a secondary problem. The charge has the ability to polarize the charge on the PCB or device. In other words, the PCB or device could have a neutral charge, but when the charged label/tape is brought into proximity it will cause the opposite charge to move to the charged label or tape. This "field induced" charge imbalance on the PCB or device creates a risk of discharge if the PCB is subsequently grounded at the inopportune time.

Figure 5: Application of PCB Label by Hand



Another concern with tapes and labels applied to a PCB occurs after application and during the life of the PCB. When the tape or label is applied to the PCB, they can be a source for charge accumulation. As mentioned previously, both the tape and label surfaces are either polyimide or have organic coatings that are inherently insulative (i.e., non-conductive). As a result, when the PCB is handled or moved—and the tape or label surface is contacted by conveyor, human, or robot—there is risk of charge building up on the surface that has the potential for enabling the polarization process described above, which in turn may lead to induction charging and discharging.

Typically, the barcode label is applied for the life of the PCB. However, in some cases, the label is removed. For example, when a PCB is made by a contract manufacturer and the PCB is shipped to another company for final assembly in a device the label may be removed. In the case for a masking tape, its function is to cover and protect an area on the PCB during assembly. At the end of the process, the tape is removed. The removal of the tape and label provides an ESD concern as charge is created during its removal. The PCB has dissimilar triboelectric charge potentials than the adhesive and thus a charge can be created on the PCB and the adhesive during removal that needs to be considered in the ESD control plan.

Countermeasures: Antistatic (Low Charging) Tapes and Labels

To address these static issues with masking tapes and/or barcode labels, an ESD control plan should consider "specialized" tapes and labels that have low-charging and static dissipative properties. Both properties will reduce the ESD risk. The following is a description of key tape and label properties and measurements.

1) Low-Charging Adhesive Systems

As mentioned earlier, a key ESD concern is the static charge that is created on the adhesive when it is removed from the liner. The dissimilar nature of the adhesive and liner allows for the adhesive to easily release, but also generates a significant triboelectric charge. To eliminate this charge build-up, there are several techniques that can be employed independently or together;

a. Matching Chemistries: By using an adhesive and liner release that are chemically similar and also closer on the triboelectric series of materials, you can decrease the charge build-up. While this is theoretically possible, it is difficult to find a system that is chemically similar and will function effectively in the application.

b. Conductive fillers: By adding conductive fillers to an adhesive, charge will move through a conductive path in the adhesive to a ground, so as charges develop, when the liner is removed, the charge is removed from the surface of the adhesive. The concern with this technology is that applying a conductive adhesive to the PCB may introduce a short or current leakage to any exposed circuits on the PCB or component.

c. Electric Field Shielding: When the liner is removed from the adhesive, the resulting charge buildup on the adhesive and liner produces an electric field that surrounds the charge. If shielding is applied in the proximity of that separation process, the charge will be reduced. The challenge with this technology is that adding shielding may not be physically possible.

When these types of features are employed in a label or tape, the resulting reduction in charge build-up on the adhesive can be significant. A common measurement method of this charge build-up is to use a static field meter to measure the electrostatic field potential at a fixed distance from the charged surface[13]. This electric field is measured in volts. Table 2 shows a comparison of charge build-up in volts for a tape adhesive with and without antistatic design features. As you can see the measured voltage of labels and tapes with antistatic features in the adhesive are significantly lower than without the features.

Table 2: Peel voltages for adhesive on a tape and label with and without low-charging features[15]

TAPE/LABEL	SIZE	LOW CHARGING FEATURE	PEEL VOLTAGE (VOLTS)
Polyimide Tape	3" x 3"	No	11,000
Polyimide Tape (w/ESD)	3" x 3"	Yes	<90
Polyimide Label	1" x 1"	No	5,000
Polyimide Label (w/ESD)	1" x 1"	Yes	<40

2) Static dissipative label face. [4,6,7,12]

After the label or tape is applied to the surface of a PCB, the insulative face can become a location for charge buildup, especially when handled and/or contacted by conveyors, etc. A key way to prevent this charge build-up is to make sure the face will allow charge movement over the surface of the tape or label and/or to a ground point. The charge movement should not be fast, but rather gradual so a large electric current is not introduced into the PCB.

The key measurement for charge movement or dissipation is the ANSI ESD STM11.11 standard test method which details the measure of surface resistance. In the standard test method, surfaces are characterized by the speed at which charges move across them as follows; conductive (rapid), dissipative (slow), or insulative (minimal/none).

The following are surface resistances that relate to the surfaces.

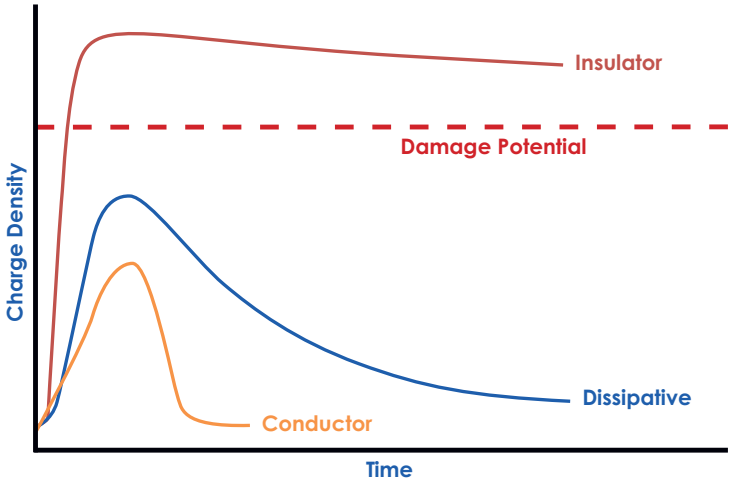
Table 3: Surface resistances for Material Types

SURFACE TYPE	CHARGE MOVEMENT	SURFACE RESISTANCE (OHM)
Conductive	Rapid	$<10^4$
Dissipative	Gradual	$>10^4$ to $<10^{11}$
Insulative	Minimal/None	$>10^{11}$

The behavior of a charge placed on these surfaces is depicted in Figure 6. If a charge is introduced to a surface by triboelectric charging, it will produce a different level of charge density that will behave differently depending on the surface type.

As noted in Figure 6, if a charge is placed on an insulative surface, it will create an immediate high charge density at the point of contact and that charge will have minimal decay over time. If an equal charge is placed on a conductive surface it will not produce a high charge density because of its rapid dissipation across the surface through electrical conduction. This rapid movement of charge can also cause damage to static sensitive devices if the current exceeds design limits. On a dissipative surface, the charge density will be initially lower than on the insulative surface and immediately begin to dissipate slowly across the surface. The dissipation speed helps prevent both high charge densities and rapid discharges and safely neutralizes the charge.

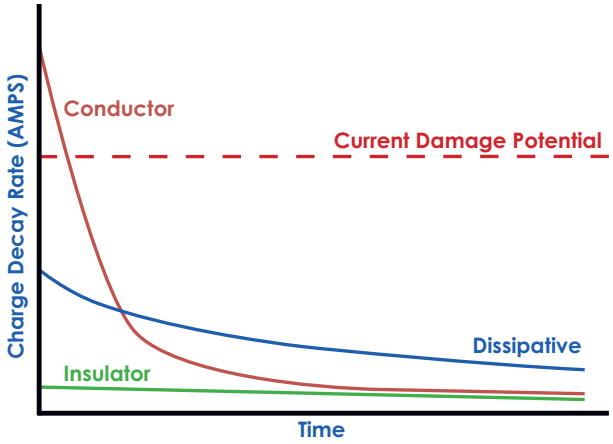
Figure 6: Static Charge Density and Decay versus Surface Type



The rate of charge movement is important. As stated previously, a rapid static discharge can be extremely destructive causing a loss of material or chemical degradation at the point of charge impact as seen in Figure 1. Secondarily, a rapid charge movement can cause degradation of a circuit. Examples include gates (switches) used in diodes and transistors which can be damaged by exposure to high voltages, reverse voltages, high current or reverse current.[16] This is often called electrical overstress (EOS). Thus, a rapid charge movement (i.e., high current) is to be avoided. (Reference Appendix 1)

The following Figure depicts the rate of charge movement (decay) for each surface type.

Figure 7: Charge Decay Rate versus Material Type



3) Low-Charging Release Liner

A third and equally important aspect of tape and label constructions that needs to be considered in an overall ESD control plan is the release liner. While the tape and label is removed and applied to the PCB, the liner also has a static charge from both the separation process of the adhesive and during handling. With respect to handling, this is often an under-considered factor in a static control plan. With either human, or machine (auto) application of the tape or label, a significant charge can be created on the liner. If not managed, the charge could be introduced into the environment and become a source of induction charging.

For the auto application of PCB labels, it is common to use a thin polyester liner to help with the fast application process. However, the polyester liner can generate significant charge. Using a liner that has a low tribocharging release coating (won't develop a charge) and is static dissipative on the back side is key to managing ESD concerns with the liner.

The following table shows the benefits of using a low-charging liner for label and tape applications by indicating the electric field potential measured on the liner and tape/labels with a static field meter.

Table 4: Static measurement for label face and liners

MATERIAL TYPE	FACE (FILM/ADHESIVE) – VOLTS	LINER – VOLTS
Polyimide Label with PET liner	12000V	8000 – 12000V
ESD Polyimide Label with ESD PET Liner	50V	50V
ESD Polyimide Label with PET Liner	40V	12000
Polyimide Label with ESD PET liner	8000V	50V

Conclusions:

Electrostatic discharge (ESD) is a major threat to meeting the short and long term performance and reliability requirements of an electronic device. During the manufacture of the device and especially during PCBA, a robust ESD control plan is an absolute requirement in order to mitigate the risk of ESD failures.

A key element of the successful ESD control plan is to manage the use of charged insulators (e.g., plastics) inside the production environment. Two common charged insulators are barcode labels and masking tapes that are widely used for tracking and protection of electronic devices, respectively. Through the use the low charging and static dissipative features on tapes and labels, the risk of ESD can be reduced.

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Gene Chase, *ESD Consultant, Electro Tech Systems*

References:

1) Fundamentals of Electrostatic Discharge; Part 3 – Basic ESD Control Procedures and Materials, ESD Association, 2014
2) How does Electrostatic Discharge (ESD) relate to Labels, Polyonics White Paper, 2003
3) Understanding and Avoiding the Costly Effects of ESD, Justin Bergholtz & Vicki Heideman, Brady Corp, June 2014
4) Thoughts on Surface resistivity Issues in ESD label materials, Jim Williams, Polyonics CTO, December 2009, internal memorandum.
5) Thoughts and comment on ESD labels, Jim Williams, Polyonics CTO, Internal memorandum.
6) Electrostatic Discharge (ESD) Properties of Plastic Packaging: Terminology, Standards, and Measurements, Scott Carter, Tek Pak Technical Bulletin.
7) Electrostatics Part 1: Electrostatic Phenomena – Principles and Measurements, Technical Report, IEC/TR 61340-1. Edition 1.0 2012-06
8) Real World Charged Board Model (CBM) Failures, Andrew Olney et al, Analog Devices
9) ESD "Best Practices", Carl Newberg, ESD Association
10) Triboelectric Generation: Getting Charged, Ryne Allen, Coping with ESD, Evaluation Engineering, 2000
11) Electro Static Discharge (ESD) – Sources of Electrostatic Charge in a SMT Production line, Hartmut Berndt, 2010 Pan Pacific Symposium Proceedings
12) ANSI/ESD S20.20 – 2014, Protection of Electrical and Electronic Parts, Assemblies and Equipment, ESDA
13) Desco Technical Bulletin TB-340, ESD Field Meter measurements, 2015 Desco Industries
14) Academy of Aerospace Quality (AAQ), ESD Damage Illustrations, JPL, aaq.auburn.edu
15) Internal Polyonics Technical Report
16) Texas Instruments, Tech Data Sheet, On-Resistance Load Switch, TPS2291, July 2015 (Appendix 1)
17) ANSI/ESD S5.3.1-2009; Electrostatic Discharge Sensitivity Testing - Charged Device Model (CDM) - Component Level
18) The Basic Principles of Electrical Overstress (EOS), OSRAM Diode, Application Note, July 2013.
19) ANSI/ESD S541-2008, Packaging Materials for ESD Sensitive Items, ESD Association Standard, September, 2008
20) ANSI/ESD STM11.11-2006: Surface Resistance Measurement of Static Dissipative Planar Materials, ESD Association, February 2007
21) ANSI/ESD ADV11.2-1995, Triboelectric Charge Accumulation Testing, ESD Association Standard, 1995

TPS2291xx, 5.5-V, 2-A, 37mΩ On-Resistance Load Switch

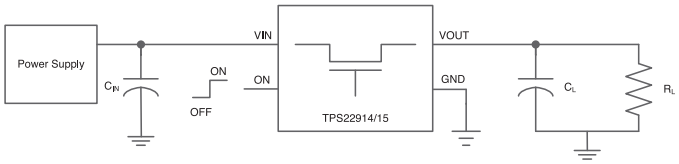
1 Features

- Integrated Single Channel Load Switch
- Input Voltage Range: 1.05 V to 5.5 V
- Low On-Resistance (R_{ON})
  - R_{ON} = 37 m (Typ) at V_{IN} = 5 V
  - R_{ON} = 38 m (Typ) at V_{IN} = 3.3 V
  - R_{ON} = 43 m (Typ) at V_{IN} = 1.8 V
- 2-A Maximum Continuous Switch Current
- Low Quiescent Current
  - 7.7 µA (typ) at V_{IN} = 3.3 V
- Low Control Input Threshold Enables Use of 1.0-V or Higher GPIO
- Controlled Slew Rate
  - t_R(TPS22914B/15B) = 64 µs at V_{IN} = 3.3 V
  - t_R(TPS22914C/15C) = 913 µs at V_{IN} = 3.3 V
- Quick Output Discharge (TPS22915 only)
- Ultra-Small Wafer-Chip-Scale Package
  - 0.78 mm × 0.78 mm, 0.4-mm Pitch, 0.5-mm Height (YFP)
- ESD Performance Tested per JESD 22
  - 2-kV HBM and 1-kV CDM

2 Applications

- Smartphones / Mobile Phones
- Ultrathin / Ultrabook™ / Notebook PC
- Tablet PC / Phablet
- Wearable Technology
- Solid State Drives
- Digital Cameras

4 Simplified Schematic



3 Description

The TPS22914/15 is a small, low R_{ON}, single channel load switch with controlled slew rate. The device contains an N-channel MOSFET that can operate over an input voltage range of 1.05 V to 5.5 V and can support a maximum continuous current of 2 A. The switch is controlled by an on/off input, which is capable of interfacing directly with low-voltage control signals.

The small size and low R_{ON} makes the device ideal for being used in space constrained, battery powered applications. The wide input voltage range of the switch makes it a versatile solution for many different voltage rails. The controlled rise time of the device greatly reduces inrush current caused by large bulk load capacitances, thereby reducing or eliminating power supply droop. The TPS22915 further reduces the total solution size by integrating a 143-Ω pull-down resistor for quick output discharge (QOD) when the switch is turned off.

The TPS22914/15 is available in a small, space-saving 0.78 mm x 0.78 mm, 0.4-mm pitch, 0.5-mm height 4-pin Wafer-Chip-Scale (WCSP) package (YFP). The device is characterized for operation over the free-air temperature range of –40°C to 105°C.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS22914B	DSBGA (4)	0.78 mm x 0.78 mm
TPS22914C		
TPS22915B		
TPS22915C		

(1) For all available packages, see the orderable addendum at the end of the datasheet.

R_{ON} vs V_{IN} (I_{OUT} = –200 mA)