Malone

Product Brief 4Kp60 HEVC Video Decoder

Multi-Format, Multi-Stream – Silicon Proven – UHD/4K – Video Decoder IP

Malone is a mature, multi-format, multi-stream video decoder which has been silicon proven on multiple STB and TV SoCs. It is a hardware decoder which is paired with a RISC controller to perform video decode. Firmware decodes stream headers, manages the decoded frames and sets up the Malone hardware. The Malone hardware fetches stream data, in either ES or PES format from external memory, decodes the pixel data and places it in external memory.

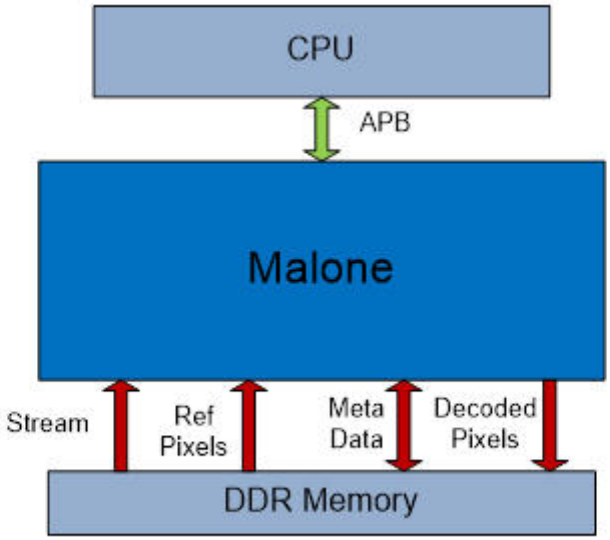

Figure 1 - Malone architecture

Formats Supported

- HEVC/H.265 MP@L5.1 (4KP60)
- H.264 AVC CBP,MP,HP up to L4.2
- H.264 MVC 1080p30 each eye
- MPEG-2 MP @ HL
- VC1/WM9 SP, MP & AP
- MPEG-4.2 SP & ASP
- MP4 (DivX3, Sorenson, H263)
- China AVS-1, AVS-P16
- RV8, RV9, RV10
- VP6, VP8
- JPEG & MJPEG up to 80Mpixes/sec
- Integrated scaler and colour space convertor

Features

- Multi-stream & Multi-format
- PES or ES stream input
- High Latency Tolerance (CPU & Memory
- Low CPU load
- Low Memory Bandwidth
- Robust Error Resilience controlled by Firmware
- Mature IP Silicon proven in multiple mass production
- STB and TV SoCs at 90nm, 45nm, 40nm & 28nm
- Production Verified Firmware
- Extensively verified with Allegro, Sarnoff and a large library of customer streams.

CS6650 FUNCTIONAL DESCRIPTION

A typical system consists of a Malone decoder, paired with a CPU, which will often be shared with other hardware blocks in the system. The Malone hardware decoder operates under the direction of firmware to perform all the computationally intensive parts of the decoding process, and provides VLD assist for firmware. Pre-decoding of headers by firmware and banking of configuration commands allows high hardware utilisation with the data path producing a single interrupt per frame, and which in turn provides high CPU latency tolerance. During multi-stream decoding only one stream will be active at any one time and switching between streams will occur at frame boundaries.

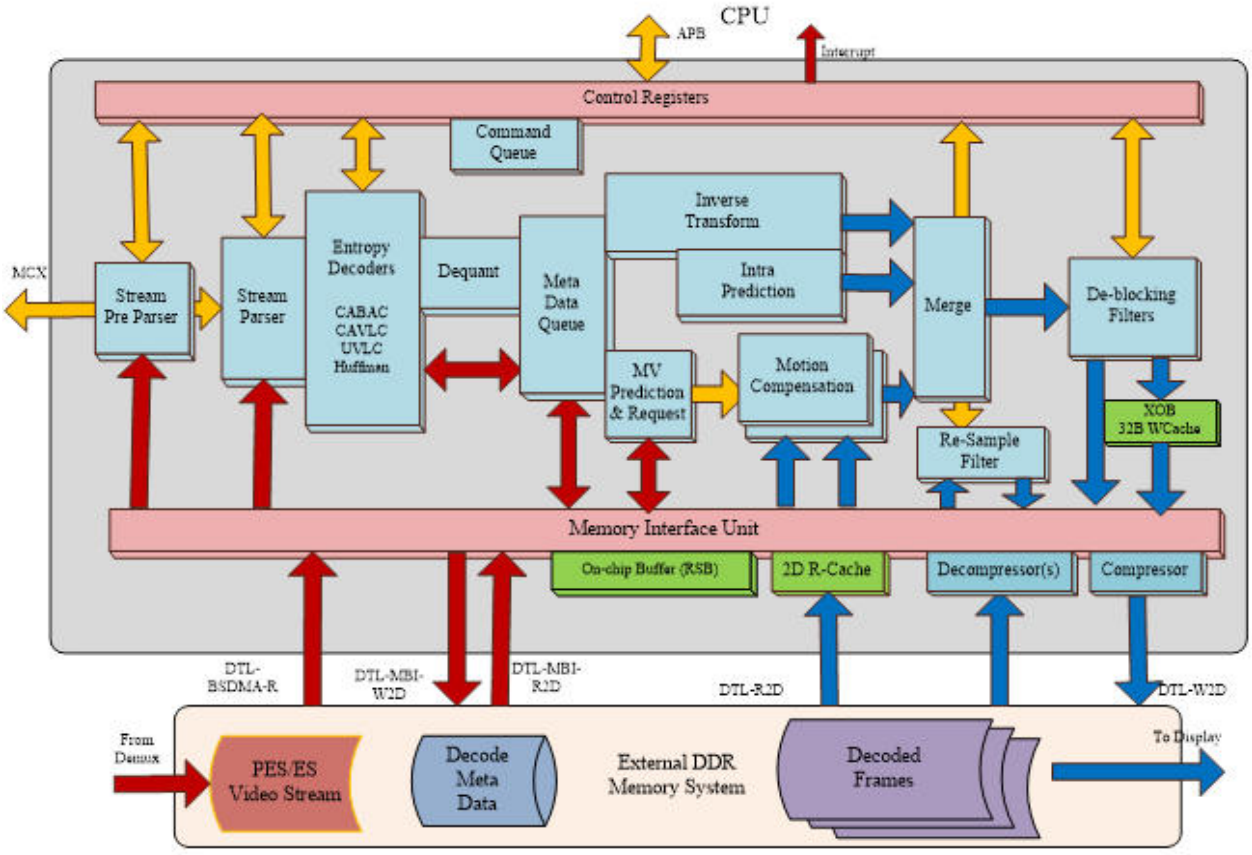

Figure 2 - Malone block diagram

DELIVERABLES

- Targeted optimized netlist for chosen technology (SoC or FPGA)
- Bit-accurate C-model
- Simulation model for system integration
- Technical support
- Test Suite (standalone self-checking test-bench which incorporates control software via PLI with reference test data)
- Synthesis scripts
- Documentation (Integration, Simulation, Application and Function databooks)

ABOUT AMPHION

Amphion is the leading supplier of silicon-proven semiconductor intellectual-property (IP) for digital video and imaging System-on-a-Chip (SoC), ASIC and programmable logic (FPGA) designs, delivering high performance solutions for video and image compression with a comprehensive range of silicon-optimized products. Amphion develops and licenses semiconductor IP cores that are close to optimal in terms of power, cycles, and area. Amphion cores operate standalone, or by in conjunction with industry-standard RISC processors, and can be easily migrated through successive generations of fabrication technology.

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