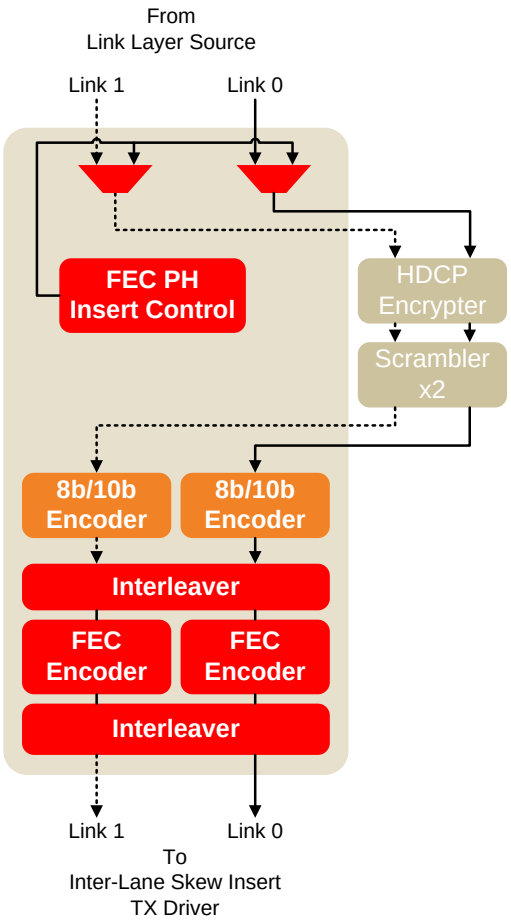
VESA DisplayPort 1.4 FEC TX IP Core

Applications

- GPUs
- Desktops & laptops
- UHD TVs and set-top boxes
- USB Type-C & DisplayPort products
- Tablets & mobiles

Hardent DP1.4 FEC TX IP



Hardent provides IP solutions as well as cutting-edge ASIC and FPGA design services for electronics manufacturers using display technology. As a member of VESA and a key contributor of the DSC Task Group, Hardent has used its expertise and skills to develop the very latest standards in display technology. Hardent's high-quality IPs enable clients to accelerate their development schedules and meet demanding time-to-market deadlines.

Description

The DisplayPort™ Forward Error Correction (FEC) Transmitter IP core implements Reed-Solomon FEC and symbol interleaving as specified by the VESA DisplayPort 1.4 specification. Forward Error Correction is required to ensure glitch-free Display Stream Compression (DSC) bitstream transport.

Key Features

- VESA DisplayPort 1.4 compliant
- Reed-Solomon (254,250) FEC, 10-bit symbols
- Two-way interleaving for 1-, 2-, and 4-lane modes (4-lane mode requires 2 FEC IP core instances)
- Optionally includes the DisplayPort main 8b/10b encoder

Deliverables

- Encrypted RTL source code IP core
- Functional and structural coverage reports
- Comprehensive integration guide
- Technical support and maintenance updates

Product Options

- IP customization and integration services available on request
- Multi-project licenses available
- UVM verification bindable modules

VESA MEMBER

Updated July 2016

Hardent
ENGINEERING | CONSULTING | TRAINING

For additional information contact:
info@hardent.com
+1-514-284-5252
www.hardent.com