Advanced Open Verification Methodology (OVM)

HDT-ADVOVM-100 (v1.0H)

Course Description

This 3-day class is designed for OVM users who have some experience with OVM but want to take their skills to the next level.

Putting together real world testbenches require more than just knowing the components of the OVM library. Real world testbenches have issues that require knowing how to apply the OVM library to solve these issues. Issues such as multiple interfaces to the DUT, layering stimulus, concurrent process synchronization, dealing with behaviors such as interrupts, resets and multiple response types, and building scalable, reusable testbenches are addressed.

In this Advanced OVM course you will gain experience in dealing with these and other testbench challenges. The class works through various testbench issues and challenges providing solutions. You will be able to apply these solutions to your testbench. You will also take away from this class detailed real world example testbenches that illustrate solutions to issues providing a great reference in doing your testbench.

This class is customized to the needs of the students.

Level – OVM 2

Course Duration – 3 days

Price – $2100

Course Part Number – HDT-ADVOVM-100 (v1.0H)

Who Should Attend? Engineers with OVM experience who want to take their skills to the next level to be able to tackle real world problems.

Prerequisites

- Introduction to OVM course or equivalent experience using SystemVerilog
- This is an advanced class and students are expected to have actual experience with the OVM library or OVM experience in addition to have taken our OVM Introductory course.

Software Tools

- Questa Simulator 10.1a+

After completing this comprehensive training, you will have the necessary skills to:

- Create scalable, reusable OVM testbench structures
- Deal with thorny issues such as reset, interrupts and synchronization across multiple components
- Apply advanced stimulus related techniques such as layered stimulus or complex scenarios
- Apply advanced analysis techniques such as scoreboard draining
- Develop a register model for your DUT and use the model for initialization and accessing DUT registers

Course Outline

- Introduction
- DUT-TB interface
- Lab – DUT-TB interface
- Container classes
  - Pools, queues
- Process Synchronization
  - Events, barriers, End of Test
- Lab - Synchronization
- Virtual Sequences
  - coordination of multiple interfaces, multiple sequencers
- Lab – Virtual sequences
- Response handling
- Interrupt handling
- Layered stimulus
- Lab – Layered stimulus
- Emulation considerations
- Coverage driven testing
- Template method pattern & OVM callbacks
- UVM Registers
  - Register model
  - Register model integration
  - Lab – Register integration
  - Register model use
  - Lab – Register use
  - Miscellaneous register topics
  - Memories

Hands-On Labs

A good proportion will be spent applying principles learned in lecture to hands-on labs.

Classroom only

This class is only taught in a classroom setting and not online

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