OVM to UVM Transition

HDT-OVMUVM-100 (v1.0H)

Course Description

This 2 day course focuses on the differences between developing testbenches with the Open Verification Methodology (OVM) and the Universal Verification Methodology (UVM). The course is taught from the viewpoint of a person who is experienced and knows OVM and is learning UVM.

Level – UVM 1

Course Duration – 2 days

Price – $1400

Course Part Number – HDT-OVMUVM-100 (v1.0H)

Who Should Attend? Engineers with OVM experience who need to learn how to use UVM.

Prerequisites

- OVM experience

Software Tools

- Questa Simulator 10.1a+

After completing this comprehensive training, you will have the necessary skills to:

- Create an UVM testbench structure using the UVM library base classes and the UVM factory
- Declare transaction items types
- Write test cases using sequences to generate stimulus for your DUT
- Develop scoreboards for analysis

Course Outline

Day 1

- Introduction to UVM
- Command Line Processor
- Phasing
- End of Test
- Configuration and Resources
- Lab - Configurations

Day 2

- UVM register model
- Register model integration
- Lab – Register integration
- Register model use
- Lab – Register use
- Example UVM testbenches

Hands-On Labs

- A good portion of class time will be spent applying principles learned in lecture to hands-on labs

Register Today

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Email: training@hardent.com
Telephone: 514-284-5252

Course material created by: