Verilog Fundamentals for SystemVerilog

HDT-VERSYSVER-100 (v1.0H)

Course Description

This 1 day course introduces engineers with "e" (Specman) or VHDL experience to the fundamentals of Verilog in preparation to learning SystemVerilog and is typically taught in conjunction with the Introduction to SystemVerilog course.

The course covers the fundamental features of Verilog in a condensed manner. It is not intended to teach Verilog design skills.

Level – SV 2

Course Duration – 1 days

Price – $700

Course Part Number – HDT-VERSYSVER-100 (v1.0H)

Who Should Attend?

- VHDL engineers who wish to learn SystemVerilog
- "e" engineers who wish to learn SystemVerilog

Prerequisites

- VHDL or "e" experience

Software Tools

- Questa Simulator 10.1a+

After completing this comprehensive training, you will have the necessary skills to:

- Learn SystemVerilog

Course Outline

- Data types
- Modules
  - Ports
  - Instances
  - Processes
  - Scheduler
  - Procedural assignments
  - Connecting and driving ports
  - Lab - Modules
- Operators
- Programming statements
- Lab - programming statements

Hands-On Labs

A good proportion will be spent applying principles learned in lecture to hands-on labs.

Register Today

Hardent offers courses to help designers produce fast predictable and efficient designs. For a detailed list, visit **www.hardent.com/training** or contact Hardent's Training Coordinator for additional information, to register for a class or to schedule a private course.

Email: training@hardent.com

Telephone: 514-284-5252

Course material created by :