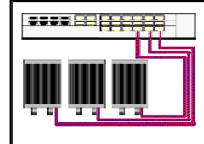




Cary Snyder
+1-360-270-4848
csnyder@ejlwireless.com



CPRI 6.0 Subsystem Technology Analysis

Optical Interfaces for Digital to RF Connectivity

December 2014



Entire contents © 2014 EJL Wireless Research LLC. All Rights Reserved. Reproduction of this publication in any form without prior written permission is strictly forbidden and will be prosecuted to the full extent of US and International laws. The transfer of this publication in either paper or electronic form to unlicensed third parties is strictly forbidden. The information contained herein has been obtained from sources EJL Wireless Research LLC deems reliable. EJL Wireless Research disclaims all warranties as to the accuracy, completeness or adequacy of such information. EJL Wireless Research LLC shall bear no liability for errors, omissions or inadequacies in the information contained herein or for the interpretation thereof. The reader assumes sole responsibility for the selection of these materials to achieve their intended results. The opinions expressed herein are subject to change without notice.

TABLE OF CONTENTS

EXECUTIVE SUMMARY	5
CHAPTER 1: CPRI TECHNOLOGY INTRO	8
Commune Radio Publica Interface Cooperantem*	8
CPRI Created to Meet Stringent Multi-RAT Requirements	10
CPRI v6.x Specification Requirements.....	11
CPRI v6.0 Changes Specific To LTE-A vs. CPRI v5.0	12
CPRI Data Rate Scaling Alters Effective Payload Data Rate	14
CRAN Wide-Area and DAS Local-Area Fronthaul.....	14
CPRI Transport Evolves Fronthaul	16
Fixing Ethernet To Handle CPRI Takes Time	21
CoE Does Not Meet Latency or Radio-Uptime Requirements	24
CPRI Networking Trends Impact Fronthaul Evolution	26
Fronthaul Using CPRI.....	27
Essential LTE-A Features and Capabilities.....	29
CHAPTER 2: CPRI SUBSYSTEM ANALYSIS.....	35
A Complex Subsystem Requirement Set	35
CPRI Subsystem Specification Changes; CPRI, sRIO, and SFP.....	35
CPRI Subsystem Outlook for 2015	40
Abstracted CPRI Subsystem Detail	43
Essential CPRI Subsystem Requirements	43
CHAPTER 3:OPEN OR VENDOR-DEFINED	44
ORI: Lack of momentum on multiple fronts	44
CPRI Subsystems: Proprietary by Design	44
CHAPTER 4: CPRI REC AND RE SoC: FPGA AND ASIC IMPLEMENTATIONS	48
CPRI FPGA/ASIC-based SoC Landscape	48
ASIC-based CPRI SoC Trend.....	49
CPRI FPGA-based SoC Landscape.....	50
CPRI v6.0 REC Bandwidth Cost Requirements.....	50
CPRI SoC Choices; Name your FPGA, ASSP, or ASIC	52
Xilinx Wireless Products Target BTS	54
Altera CPRI Devices and IP.....	57
FPGA-based CPRI v6.x Subsystem Market Demand in 2015.....	59
FPGA Design and IP Validation Methodology and Process	63
Developing CPRI Subsystem ASIC/SoC Trends.....	65
CHAPTER 5: CPRI SUBSYSTEM IP	67
CPRI SoC and Subsystem IP; Wild Mix of IP	67
CHAPTER 6: CPRI SUBSYSTEM DESIGN	70
ASIC/FPGA Simulation, Emulation, Prototype Bring-Up	70
Game Changing CPRI Subsystem Testing.....	72
CHAPTER 7: CPRI SUBSYSTEM TEST ECOSYSTEM.....	75
CPRI v6 is a Stress Test Focal Point.....	77
CPRI /Fronthaul Jitter: The 2015 Lighting Rod	78
CHAPTER 8: sRIO/BBU FABRIC DATAFLOW	79
RapidIO.org Embedded Switch Fabric Summary.....	79
Integrated Devices Technology (IDT) sRIO Products	80
sRIO v3.1 Spec Aligns with CPRI v6.x Spec/Requirements	82
CHAPTER 9: SFP/SFP+ FOR CPRI.....	84
SFP/SFP+ Optical Module Support.....	84
CPRI SFPs require BTS Certification.....	85
SFP Probing and Diagnostics	87

TABLES

Table 1: Comparing Common Elements of CPRI to OBSAI	9
Table 2: Comparison of LTE TDD and FDD Technologies.....	10
Table 3: Network Uptime Availability Standards	10
Table 4: CPRI v6.0 Specification Requirements	11
Table 5: 3GPP LTE-A Specification Differences Between CPRI v5.0 and CPRI v6.0	12
Table 6: Metro Ethernet Forum Mobile Backhaul IA, Phase 2, Amendment 1	19
Table 7: Current and Next Generation Mobile Fronthaul Requirements.....	26
Table 8: New mobile timing-synchronization requirements for 3GPP Release 12.....	29
Table 9: Required CPRI LTE BW per Radio Head (RH) to match ≤ 2.4576 Gbit/s	31
Table 10: Required CPRI LTE BW per Radio Head (RH) to match ≤ 6.144 Gbit/s	32
Table 11: Required CPRI LTE BW per Radio Head (RH) to match ≥ 6.144 Gbit/s	33
Table 12: Comparing Ethernet vs. RapidIO Technology	37
Table 13: sRIO v3.1 Spec Means CPRI Subsystem Redesigns	38
Table 14: CPRI SoC Subsystem ASIC Vendors	48
Table 15: Primary ASIC and FPGA, and IP Vendor Companies for BTS OEMs.....	48
Table 16: Typical CPRI line, payload, and compressed data rates shipping in 2014.....	50
Table 17: CPRI SoC Subsystems; FPGA Prototype to FPGA and ASIC Production	52
Table 18: CPRI SoC Subsystems; FPGA Prototype to FPGA and ASIC Production	53
Table 19: Altera's CPRI SoC Device Choices	57
Table 20: Comparing CPRI v4.x, v5.0, and v6.x For LTE-A Release 12/14 Support.....	61
Table 21: Current CPRI v5.0 Subsystem use of Gen 2 sRIO Technology	63
Table 22: Next Generation 3GPP Fronthaul Roadmap.....	66
Table 23: Niche IP for BTS and CPRI Subsystem Development.....	67
Table 24: CPRI Subsystem IP Vendor	68
Table 25: Compression IP Products, IDT's I2Q and Altera's Compression IP notation	69
Table 26: BTS CPRI Subsystem IP and Test Vendor Overview.....	70
Table 27: CPRI Subsystem Test Products	75
Table 28: RapidIO.org Membership 2014 compared to 2005.....	79
Table 29: IDT's sRIO Roadmap through 2015	81
Table 30: sRIO v3.1 Timing, Fault/Error Tolerance, and Diagnostic Enhancements	82
Table 31: Recently Updated SFP/QSFP Docs to include Diagnostic Monitoring Interface.....	86
Table 32: SPF/SPF+ Vendor use of I2C/2-wire programming interface and diagnostic monitoring	87
Table 33: New Specifications for Diagnostic Monitoring	87
Table 34: Diagnostic Monitoring Types.....	89
Table 35: Enhanced Monitoring Options	89
Table 36: Diagnostic Flag Alarm and Warning Thresholds.....	89
Table 37: Diagnostic Calibration Constants for External Calibration	90
Table 38: Diagnostics Diagnostic Monitor Data (Internal or External).....	90
Table 39: Optional Status/Control Bits	90
Table 40: Address 112 Temp, Vcc and TX Diagnostic Alarm Flags Status Bits	90
Table 41: Address 113 RX Diagnostic Alarm Flags Status Bits	91
Table 42: Address 114 Diagnostic Alarm Status Bits	91
Table 43: Address 115 Diagnostic Alarm Status Bits	91
Table 44: Address 116 Temp, Vcc and TX Diagnostic Warning Flags Status Bits	91
Table 45: Address 117 RX Diagnostic Warning Flags Status Bits	91
Table 46: Address 118 Extended Module Control and Status Bits	92
Table 47: Address 119 Extended Module Control and Status Bits Status Bits	92
Table 48: Address 120-127 Vendor Password	92
Table 49: Address 128-255 User EEPROM and Vendor Control Functions.....	92

EXHIBITS

Exhibit 1: CPRI Specification as applied to BTS, Fronthaul and Backhaul	5
Exhibit 2: CPRI Ecosystem Diagrams, <i>Simple B&W To Complex with Color</i>	8
Exhibit 3: Impact of Multiple Fiber Hop Scenario on CPRI Signal	15
Exhibit 4: Existing Fiber Optic Routing Model Example	16
Exhibit 5: Practical C-RAN Ring Routing Example	16
Exhibit 6: Practical C-RAN Ring Routing Example	17
Exhibit 7: Alcatel-Lucent/TE Connectivity DAS Example	20
Exhibit 8: Ericsson's Use of CPRI for Fronthaul.....	21
Exhibit 9: CPRI CoOp to Help IEEE TSN Fix Ethernet To Carry CPRI	23
Exhibit 10: Can the CPRI CoOp Help IEEE TSN Replace DWDM With Ethernet?.....	23
Exhibit 11: IEEE Project 1904.3 – Radio over Ethernet (RoE).....	24
Exhibit 12: Comparison of throughput and latency: sRIO vs. PCIe vs. Ethernet.....	25
Exhibit 13: Ethernet and Optical Module Roadmap	26
Exhibit 14: Alternatives to CPRI-Fronthaul	27
Exhibit 15: CPRI v6.x Substantially Increases Data Payload Rate with 64b/66b Encoding	28
Exhibit 16: CPRI Subsystem Drawing	30
Exhibit 17: CPRI Subsystem Clock Circuitry To Control Timing, Jitter, and Phase Sync.....	31
Exhibit 18: CPRI v6.0 Subsystem support for LTE-A 3GPP Release 12.....	34
Exhibit 19: Tightly Coupled Coordination Complicates CPRI Subsystem Design	35
Exhibit 20: CPRI Subsystem Architecture: Processing Blocks and Testable IP Links	36
Exhibit 21: CPRI Spec Diagram with Network Interface Detail.....	39
Exhibit 22: CPRI Subsystem Deployment Roadmap for 2015 and beyond.....	40
Exhibit 23: LTE-A Peak Data Rate Evolution	42
Exhibit 24: CPRI-based Subsystems with Multiple Master and Slave SoCs	45
Exhibit 25: Small Cell Forum Plugfests' attempt to standardize CPRI/RRH IoT.....	47
Exhibit 26: CPRI Subsystem "Hot Ring", Star, and Chain RRH topologies	49
Exhibit 27: Typical CPRI Subsystem "Hot Ring" topology.....	49
Exhibit 28: BTS CPRI v6.0 Subsystem requires 72Gbps to 100Gbps	50
Exhibit 29: BTS CPRI Subsystem SoC Interfaces; Standardized CPRI DU/RRH Links	51
Exhibit 30: BTS CPRI Subsystem Requirements Roadmap to 2025	53
Exhibit 31: Xilinx's CPRI Subsystem SoC, with Dual-ARM Core with High-Speed I/O	54
Exhibit 32: Xilinx's CPRI Subsystem RE SoC Functions.....	55
Exhibit 33: CommAgility Kintex-based Prototype and Specialized Radio Product Platforms	55
Exhibit 34: Altera Stratix V Prototype Kit with "Design Suite" Tools	56
Exhibit 35: Altera Stratix V Prototype Platform	56
Exhibit 36: Arria 10 CPRI and sRIO Transceiver HW and IP support.....	57
Exhibit 37: Altera's CPRI and CPRI Subsystem Priority Wanes	59
Exhibit 38: AMC Altera FPGA-based CPRI v6.0 SoC Dev board	59
Exhibit 39: CPRI Layer 1 REC to RE Link	62
Exhibit 40: CPRI/SFP+ Development Boards from HiTech Global	64
Exhibit 41: CPRI FPGA Dev Boards from S2C (left) and Mercury Systems (right).....	64
Exhibit 42: BTS CPRI Subsystem "Data Rate" Requirements Roadmap to 2015.....	66
Exhibit 43: BTS CPRI Subsystem IP Overview.....	67
Exhibit 44: Representation of RapidIO Switch Fabric Role in BTS CPRI Subsystems	71
Exhibit 45: Base Transceiver Station System/CPRI Subsystem Test System	71
Exhibit 46: Sarokal X-STEP Test System Product Overview	72
Exhibit 47: Pre-Silicon Capture of JESD203 Test Vectors.....	72
Exhibit 48: BTS system and CPRI Subsystem ASIC/FPGA Design Support	74
Exhibit 49: CPRI v6.x Subsystem/System-Level Simulation and Test Configuration	77
Exhibit 50: Traditional Test Probing vs. Extended X-STEP Probing	77
Exhibit 51: Current state of CPRI Subsystem Jitter.....	78
Exhibit 52: Can the CPRI CoOp replace DWDM with Ethernet?	78
Exhibit 53: BTS Digital Unit (DU) currently use Gen 2 sRIO Switch Chips	80
Exhibit 54: Adaptable CPRI/OBSAI Subsystem PHY and Optical Transceiver Options.....	84
Exhibit 55: SFP+ Digital Diagnostic Monitoring enhanced by SFF MSA Work	85
Exhibit 56: SFF-8472 SFP+ Digital Diagnostic Memory Maps (A0h and A2h)	88
Exhibit 57: SFP+ SCL-SDA Digital Diagnostic Schematic and Footprint.....	93