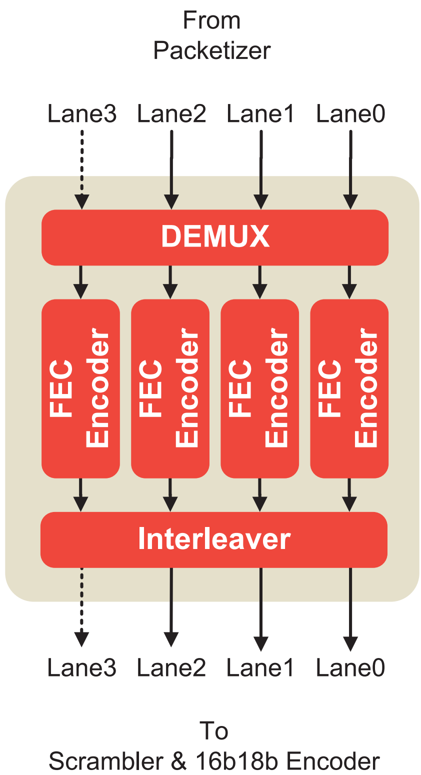
HDMI 2.1 FEC TX IP Core

Applications

- GPUs
- Desktops & laptops
- UHD TVs & set-top boxes
- Professional video equipment

Hardent HDMI 2.1 FEC TX IP



Hardent's IP portfolio offers customers ready-made solutions to accelerate product development and meet demanding time-to-market schedules.

Developed by a team of experienced FPGA and ASIC designers, Hardent's IP cores have undergone extensive verification and offer proven interoperability and compatibility.

Description

The HDMI Forward Error Correction (FEC) Transmitter IP Core implements Reed-Solomon FEC and symbol mapping/interleaving as specified by the HDMI 2.1 specification.

Forward Error Correction is required to ensure glitch-free operation in Fix Rate Lane (FRL) mode, a packet mode introduced in HDMI 2.1. FRL allows for the use of Display Stream Compression (DSC) bitstream transport.

Key Features

- HDMI 2.1 compliant
- Reed-Solomon RS(255,251) FEC, 8-bit symbols
- Supports 3-lane and 4-lane operation

Deliverables

- Encrypted RTL source code IP core
- Functional and structural coverage reports
- Comprehensive integration guide
- Technical support and maintenance updates

Product Options

- IP customization and integration services available on request
- Multi-project licenses available
- UVM verification bindable modules

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