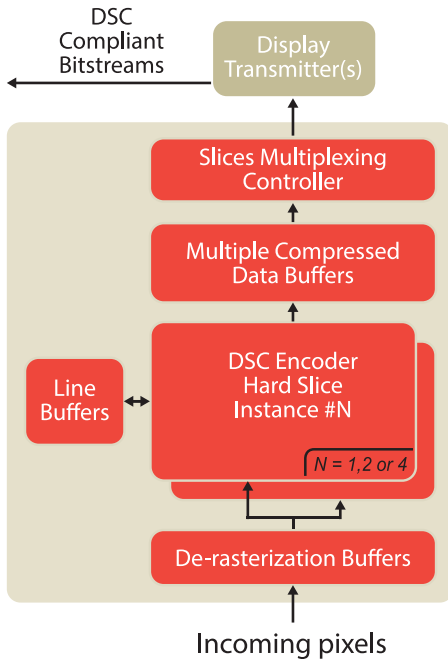# VESA DSC 1.2a
Encoder
IP Core

Applications

- 4K / 8K / UHD TVs
- Digital TV products
- AR / VR products
- DisplayPort 1.4 products
- USB Type-C products
- HDMI 2.1 products

Hardent DSC Encoder IP

DSC Compliant Bitstreams ← Display Transmitter(s) ← Slices Multiplexing Controller ← Multiple Compressed Data Buffers ← DSC Encoder Hard Slice Instance #N (N = 1, 2 or 4) ↔ Line Buffers ← De-rasterization Buffers ← Incoming pixels

Key Features

- VESA Display Stream Compression (DSC) 1.2a compliant
- Supports all DSC 1.2a mandatory encoding mechanisms
  - MMAP, BP, MPP, and ICH
- Output buffering compatible with transport stream over video interfaces
- Configurable maximum display resolution
  - Up to 4K (4096x2160), 5K (UHD+), and 8K (FUHD)
- 8, 10, 12, 14, and 16 bits per video component
- YCbCr and RGB video input format
- 4:4:4, 4:2:2, and 4:2:0 native coding
- 1 pixel / clock internal processing architecture in 4:4:4
- 2 pixels / clock internal processing architecture in 4:2:2 and 4:2:0
- Parameterizable number of parallel slice encoder instances (1, 2, or 4) to adapt to the capability of the technology and target display resolutions used
- Multiple slices per line in each encoder instance supported
- 100% verification coverage based on UVM environment
- Verified against the VESA DSC 1.2a C model using a comprehensive test image library
- Backward compatible with DSC 1.1

Deliverables

- Encrypted RTL source code IP core
- Functional and structural coverage reports
- Comprehensive integration guide
- Technical support and maintenance updates

Product Options

- IP customization and integration services available on request
- Multi-project licenses available
- UVM verification bindable modules

Hardent's IP portfolio offers customers ready-made solutions to accelerate product development and meet demanding time-to-market schedules.

Developed by a team of experienced FPGA and ASIC designers, Hardent's IP cores have undergone extensive verification and offer proven interoperability and compatibility.

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