Intel Stratix 10 SX SoC Dual FMC+ Development Platform Product Brief (HTK-S10Sx-DFMCP)

Features

- Intel S10 SX SoC FPGA (L or H Transceiver Tiles)
- Signal Processing and wireless communications centric design
- Dual FMC plus mezzanine slots for application scalability and flexibility
- Compact 8.15” x 8.4” module
- Complete FPGA support package available
- Rich suite of Ethernet IP cores available
- Available as integrated 19” half width, 1U, 300mm deep standalone SoC FPGA device

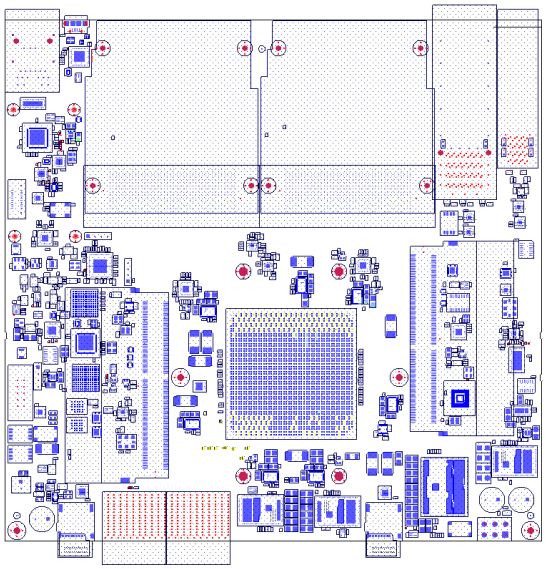
Applications

- Rapid prototyping
- Volume production with Stratix 10 SX SoC FPGA
- OEM and white label devices and platforms

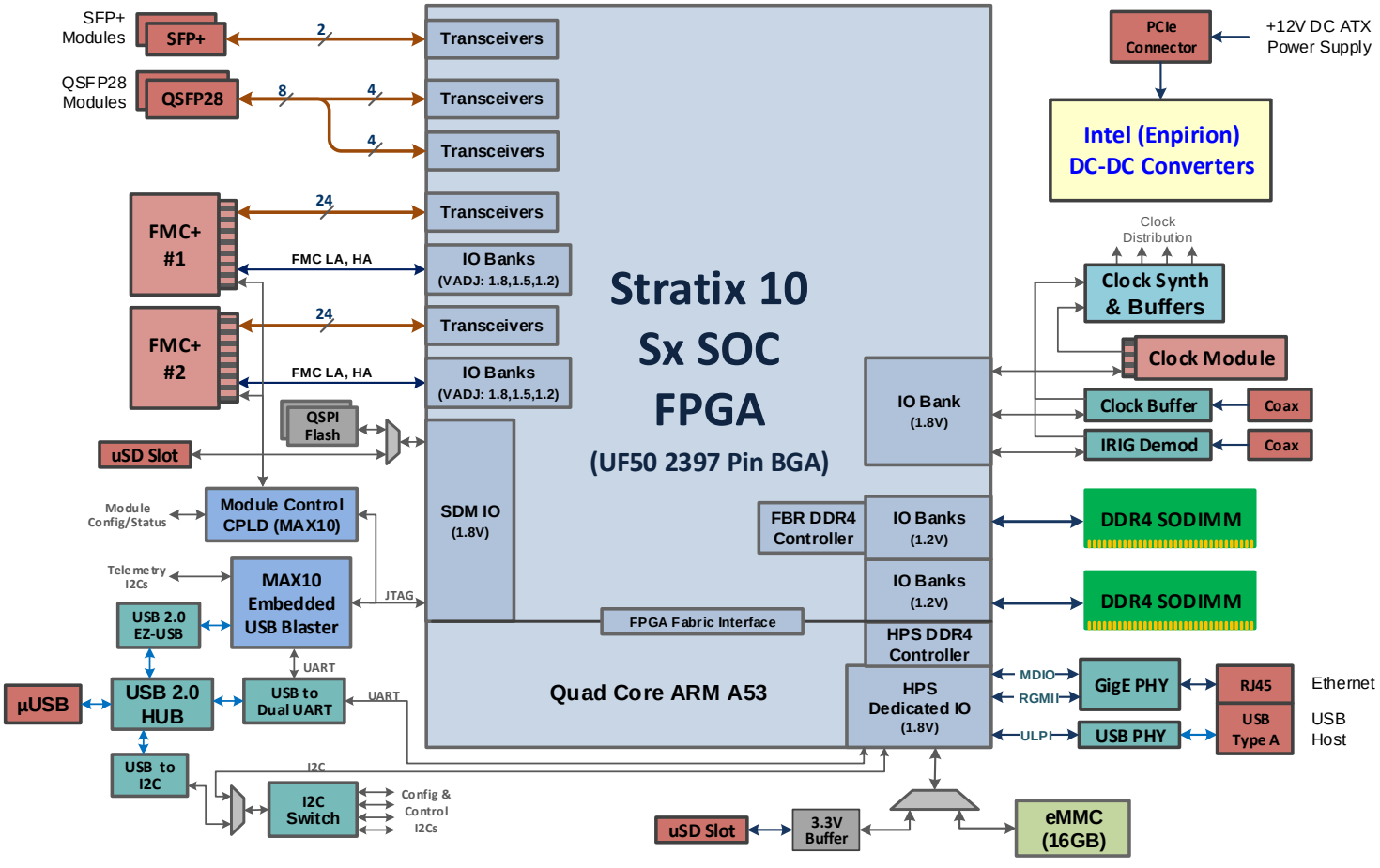
Target Markets

- Wideband Wireless and RF Communications
- 5G wireless technology development
- Signal Processing / Image Processing
- 10G/25G/40G/100G networked signal processing devices and platforms

HIGHLY INTEGRATED, SCALABLE, FEATURE RICH, SIGNAL PROCESSING CENTRIC DEVELOPMENT PLATFORM



The Intel Stratix 10 SX (up to Sx2800) SoC FPGA based development platform for signal processing and communication centric designs with dual FMC+ mezzanine slots, dual QSFP28 and dual SFP+ front panel interfaces. Integrated quad-core 64-bit A-53 ARM processor complex with network, control and storage peripherals.



HTK-S10Sx-DFMCP

Front Panel Interfaces

- Dual FMC+ (Vita 57.4) mezzanine interfaces. All 34 LA diff-pairs, 24 HA diff-pairs and 24 Serdes lanes routed to FPGA. Backwards compatible with FMC (Vita 57.1) modules.
- Max VADJ of 1.8V on LA, HA signals; DIP switch selectable for 1.2V, 1.5V and 1.8V
- Dual QSPF28 ports for 2x100G, 2x40G, 8x25G and 8x10G data plane network interfaces
- Dual SFP+ ports for 10G/1G for control plane network interface to A-53 ARM controller
- Micro-USB 2.0 control and configuration port with integrated USB hub for single cable access to integrated USB Blaster II, module management and serial debug console
- RJ45 GigE and USB2.0 host interface to A-53 ARM controller HPS

Fabric Memory and SDM Configuration Interfaces

- One 64-bit DDR4 SODIMM slot with dual-rank and dual-die support
- SDM configuration options for QSPI, microSD and JTAG
- Dual 512Mbit Micron QSPI Flash memory device boot
- MicroSD slot for FPGA configuration through microSD plug-in memory card

HPS Memory Interfaces

- One 64-bit DDR4 SODIMM slot with dual-rank and dual-die support
- On-board slot for uSD memory card
- On-board 16Gbyte eMMC storage device

Power Tree

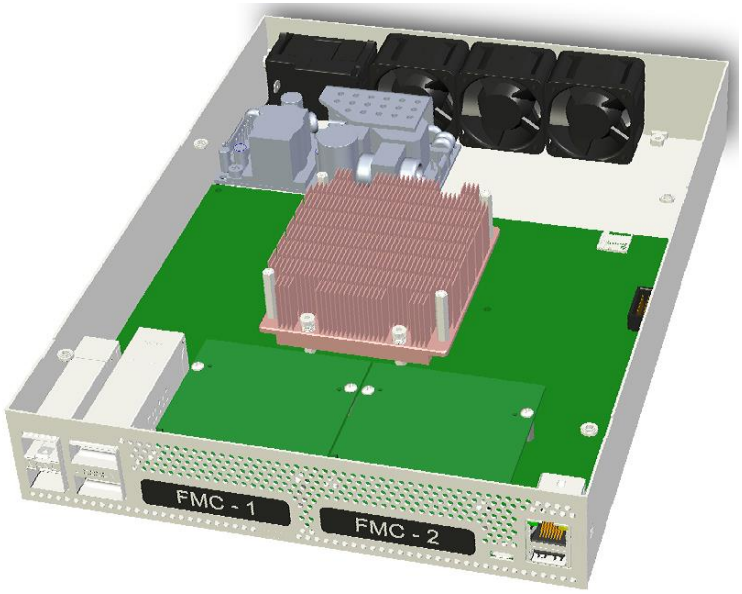
- ***All Intel (Enpirion) power tree*** conforming to Intel's recommended Stratix10 power-up and power-down sequencing
- ATX power supply (PCIe) 12V power connecter
- Remote power management through USB console

Clock and Synchronization functions

- 5–200MHz external reference clock input
- 1PPS or IRIG-A/B/G (DCLS and AM) input
- Flexible clocking tree with Silicon lab Si5345 clock de-jitter and synthesizer
- Flexible FMC+ clock routing and configuration
- Support for application specific clocking including GPS interface through clock mezzanine module

On-board Development and Debug Support

- Integrated USB Blaster II
- Remote module management and control for power, boot and reconfiguration through USB interface
- Module clock configuration management through HPS I2C interface
- Temperature monitor and power modules telemetry through USB interface
- Automatic over-temp shut down
- Multiple on-board and front panel diagnostic and status LED's



Low cost, quick turnaround customizations available

Links

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