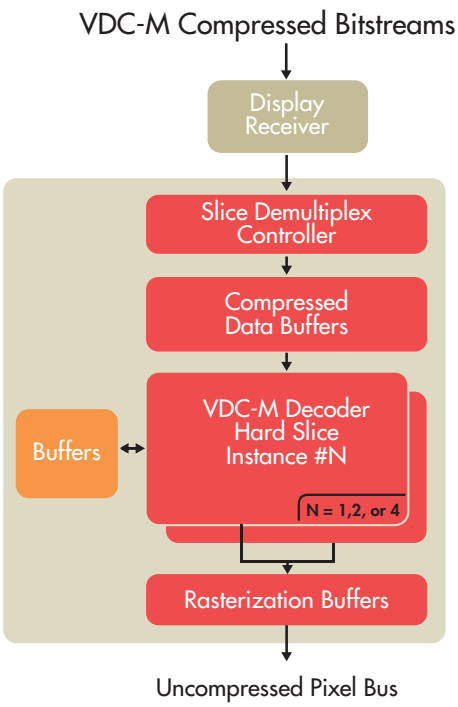
VESA VDC-M 1.1 Decoder IP Core

Applications

- Mobiles & Tablets
- AR/VR Products
- MIPI DSI-2 Applications
- Automotive Video Transmission

Hardent VDC-M 1.1 Decoder IP Core



Hardent's IP portfolio offers customers ready-made solutions to accelerate product development and meet demanding time-to-market schedules.

Developed by a team of experienced FPGA and ASIC designers, Hardent's IP cores have undergone extensive verification and offer proven interoperability and compatibility.

Description

The Hardent VESA VDC-M 1.1 Decoder IP Core implements a fully compliant VESA Display Compression-M (VDC-M) 1.1 decoder to deliver visually lossless video compression. The decoder supports various usage models, including typical MIPI Display Serial Interface 2 (MIPI DSI-2) usage models.

Key Features

- VESA Display Compression-M (VDC-M) 1.1 compliant
- Supports all VDC-M encoding mechanisms
  - o BP, transform, MPP, MPP fallback, and BP skip
  - o Flatness detection and signalling
- Configurable maximum display resolution of up to 16Kx16K
  - o Typical 4K (4096x2160), 5K UHD+, and 8K UHD supported
- 8, 10, or 12 bits per component video
- 4:4:4 samples for RGB video output format
- 4:4:4, 4:2:2, and 4:2:0 samples for YCbCr video output formats
- Parameterizable number of parallel slice decoder instances (1,2 or 4) to adapt to the capability of the technology and target display resolutions used
- Supports logical slice decoding (soft slice) in each physical decoder (hard slice)
- Ultra-low latency
- Pixel throughput of four pixels per clock per hard slice decoder
- Optimized for power saving

Deliverables

- Encrypted RTL source code IP core
- Functional and structural coverage reports
- Comprehensive integration guide
- Technical support and maintenance updates

Product Options

- IP customization and integration services available
- Multi-project licenses available

VESA MEMBER

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