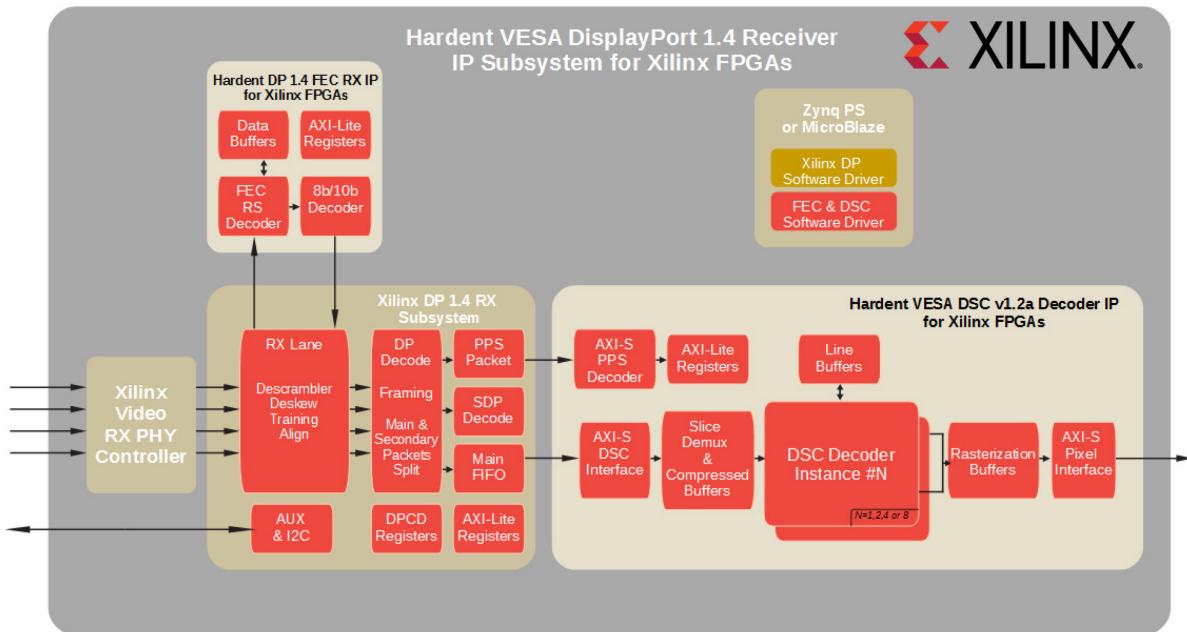


VESA DisplayPort 1.4 RX IP Subsystem for Xilinx FPGAs

Applications

- 4K / 8K Monitors
- Digital Signage
- Video Converters
- Projectors
- Multiviewers



Key Features

- Complete DisplayPort™ 1.4 Receiver solution with support for VESA Display Stream Compression (DSC)
- Fully compliant with the DisplayPort 1.4a Standard
 - Including the DSC slices per line requirements
- Supports up to **4 lanes at HBR3 rate (8.1 Gbits/sec)**
- Configurable maximum display resolution up to **8K (FUHD) 60fps in RGB 444**
- All color spaces supported by DSC v1.2a and component bit depth up to 12 bits
- Support for **Xilinx® UltraScale™ and UltraScale+™** devices

Deliverables

- Xilinx Video PHY Controller & DisplayPort 1.4 RX Subsystem IP
- Hardent VESA DisplayPort 1.4 Forward Error Corrector (FEC) Receiver IP for Xilinx FPGAs
- Hardent VESA Display Stream Compression (DSC) 1.2a Decoder IP for Xilinx FPGAs
- Reference design with Vivado® Design Suite & SDK project files
- Documentation for each Hardent IP core
- Comprehensive integration guide
- Software drivers and user application example
- Technical support from Hardent included

Hardent's IP portfolio offers customers ready-made solutions to accelerate product development and meet demanding time-to-market schedules. Developed by a team of experienced FPGA and ASIC designers, Hardent's IP cores have undergone extensive verification and offer proven interoperability and compatibility.

