SV4E-DPTXCPTX
MIPI Transmit Device Emulator
PRODUCT BRIEF

System-Level Tester for Exercising and Validating MIPI Devices

Figure 1. Introspect's compact SV4E-DPTXCPTX system-level tester (140 mm x 89 mm)

The SV4E-DPTXCPTX is a highly integrated system-level tester that facilitates the rapid screening, calibration, and optimization of MIPI® Alliance enabled devices. Such devices include high-resolution display panels or display driver ICs, advanced image signal processors, and microcontrollers used in mobile or IoT applications. The SV4E-DPTXCPTX features a unique dual-mode D-PHY℠/C-PHY℠ analog front-end. It also integrates reconfigurable protocol stacks for the DSI℠, DSI-2℠, and CSI-2℠ standards. These features make it incredibly easy to create a realistic test setup for tuning and calibrating system parameters such as display color settings or power performance.

FEATURES

- **Dual-mode PHY:** software configurable to act as a D-PHY or a C-PHY transmitter
- **High bandwidth:** up to 4.5 Gbps D-PHY signaling and 2.5 Gsps C-PHY signaling per lane; up to 4 lanes per port
- **Native protocol implementation:** true CSI-2, DSI, and DSI-2 controller instantiations include escape-mode capability and bus turnaround (BTA)
- **Easy to use:** Introspect ESP Software enables interactive operation or full automation

BENEFITS

- **Future proof:** protect your investment by adopting a single tool for multiple product applications and across a large span of data rates
- **Self-contained:** an all-in-one system enables true protocol handshake and helps create a system-oriented testing methodology
- **Automated:** scripting capability is ideal for debug tasks, firmware verification, and full-fledged production screening of devices and system modules

Typical Application: DDIC Protocol and Packet Exercising

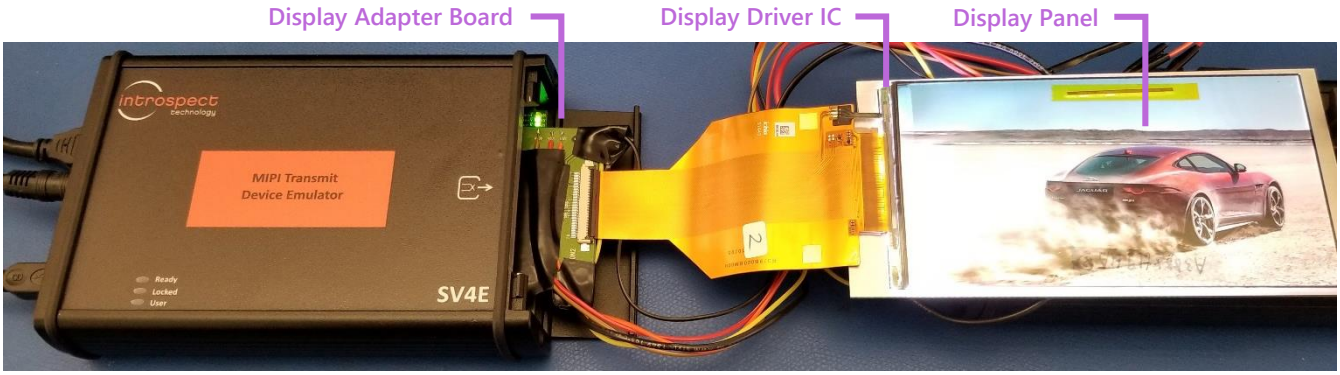

Figure 2. SV4E-DPTXCPTX testing a C-PHY liquid crystal module

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Protocol and Transmission Parameters

Feature	Description	Benefit
Application / Protocol Support	D-PHY version 1.1, 1.2, 2.0 (including BTA) C-PHY version 1.0, 1.2 (including BTA) CSI-2 version 1.3, 2.0, 2.1 DSI version 1.3, 1.3.1 DSI-2 version 1.0, 1.1 DSC version 1.1, 1.2	Allows for flexible stimulus generation and varied application contexts including ADAS sensors, small format displays, and large format displays
Transmission Payload Support	PRBS packet loop patterns HS-only and LP-only patterns Arbitrary video patterns at any frame rate Colour bar patterns at any frame rate	Provides a wide spectrum of stimulus conditions for the purposes of debug or colour calibration during production

Key Performance Parameters

Parameter	Value	Description
Lane Count	4 lanes of D-PHY; 4 lanes of C-PHY	Allows for deployment into multiple generations of products or multiple product families
Data Rates	80 Mbps to 4.5 Gbps in D-PHY mode; 80 Msps to 2.5 Gsps in C-PHY mode	Allows for supporting high-performance applications
GPIO	DUT reset control pin Tearing effect trigger pin 14 user programmable IO pins	Provides full control over devices under test
Auxiliary Power	Up to 6 DC outputs with CMU capability	Enables complete module test and DC measurement capability

Single component representing the tester's top level

DSI/DSI-2 frame generation with arbitrary pixel formats and display stream compression

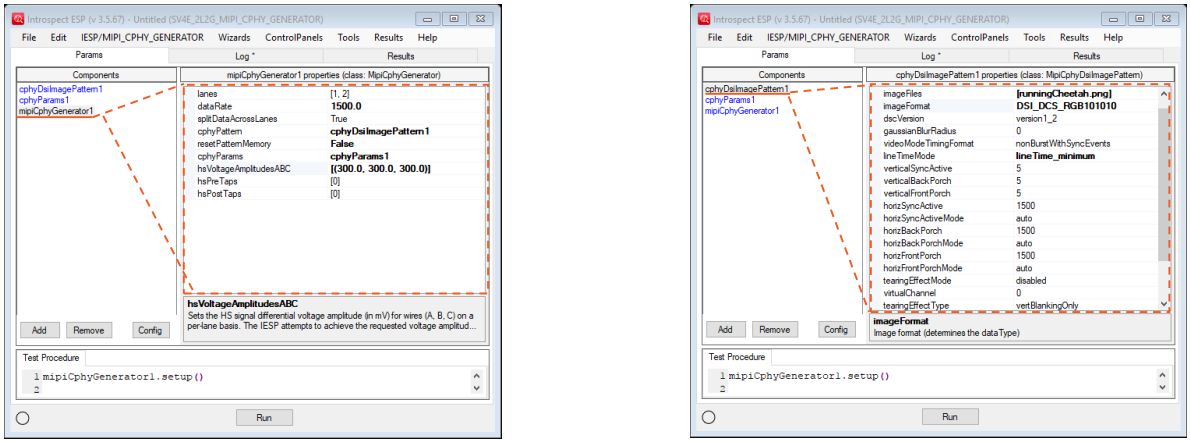

Figure 3. Introspect ESP Software offers the most rich usage and deployment experience for the SV4E-DPTXCPTX