Hardent Lossless Video Compression (HLVC)
Decoder IP Core

File I/O or Transport Interface → File or Transport Container → Optional AXI-S Interface → Multiple Compressed Data Buffers → Channel #N Lossless Decoder (N = 1,2,3, or 4) ↔ Context Buffers → Data Post-Processing & Re-Ordering → Outgoing Sensor RAW Data or Post-Processed Data
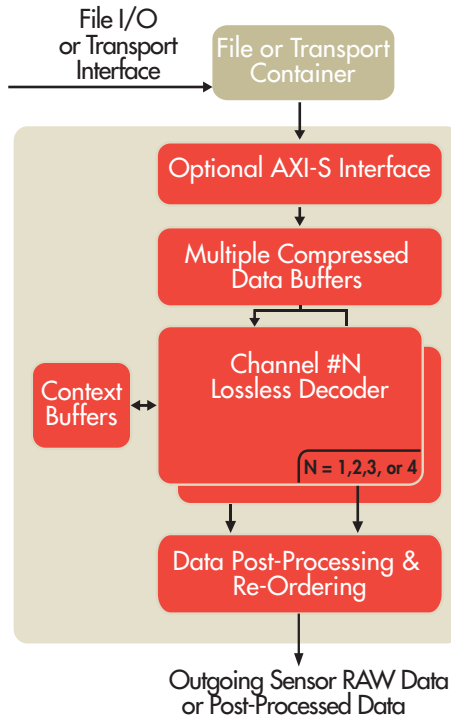
Key Features

- True mathematically lossless (bit-exact) compression
- Supports lossless compression of a wide variety of RAW data
  - Image sensor RAW data Color Filtered Array (CFA)
  - Monochrome
  - GRGB, RGBE, RCCG, RCCC
  - Metadata such as XMP, Exif
  - Post-processed data such as disparity maps from 3D sensors
- Low complexity hardware implementation
- Ultra-low latency performance
- Parameterizable number of parallel channels (components)
- Configurable to any sensor resolution
- Configurable (per channel) bit depth: 8, 10, 12, 14, 16 bits and higher (32 bits & 64 bits also supported)
- Configurable Transfer Unit (TU) to adapt to file or transport container
- Both FPGA and ASIC implementations available with real-time encoding capabilities
- 100% verification coverage based on UVM environment

Deliverables

- Bit exact reference software model
- Encrypted RTL source code or FPGA netlist IP core
- Functional and structural coverage reports (for ASIC)
- Design specification & comprehensive integration guide
- Technical support and maintenance updates

Product Options

- Real-time / faster than real-time software codec
  - Optimized for x86 or ARM CPU architectures
  - Leverages SIMD instruction set
  - OS-specific API (Windows / Linux) available on request
  - Optionally, a GPU fragment shader can be leveraged to lower CPU requirements
- IP customization and integration services available on request

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