XILINX

Designing with the Versal ACAP: Architecture and Methodology

ACAP 1

ACAP-ARCH (v1.0H)

Course Specification

Course Description

This course helps you to learn about Versal™ ACAP architecture and design methodology.

The emphasis of this course is on:

- Reviewing the architecture of the Versal ACAP
- Describing the different engines available in the Versal architecture and what resources they contain
- Utilizing the hardened blocks available in the Versal architecture
- Using the design tools and methodology provided by Xilinx to create complex systems
- Describing the network on chip (NoC) and AI Engine concepts and their architectures
- Performing system-level simulation and debugging

Level – ACAP 1

Course Duration – 3 days

Price – $2700 or 27 Training Credits

Course Part Number – ACAP-ARCH

Who Should Attend? – Software and hardware developers, system architects, and anyone who wants to learn about the architecture of the Xilinx Versal ACAP device

Prerequisites

- Comfort with the C/C++ programming language
- Vitis™ IDE software development flow
- Hardware development flow with the Vivado® Design Suite
- Basic knowledge of UltraScale™/UltraScale+™ FPGAs and Zynq® UltraScale+ MPSoCs

Software Tools

- Vivado Design Suite 2020.2
- Vitis unified software platform 2020.2
- PetaLinux Tools 2020.2

Hardware

- Architecture: Xilinx Versal ACAPs

After completing this comprehensive training, you will have the necessary skills to:

- Describe the Versal ACAP architecture at a high level
- Describe the various engines in the Versal ACAP device
- Use the various blocks from the Versal architecture to create complex systems
- Perform system-level simulation and debugging
- Identify and apply different design methodologies

Course Outline

Day 1

- **Introduction**

  Talks about the need for Versal devices and gives an overview of the different Versal families. {Lecture}
- **Architecture Overview**

  Provides a high-level overview of the Versal architecture, illustrating the various engines available in the Versal architecture. {Lecture}
- **Design Tool Flow**

  Maps the various engines in the Versal architecture to the tools required and describes how to target them for final image assembly. {Lecture, Lab}
- **Adaptable Engines (PL)**

  Describes the logic resources available in the Adaptable Engine. {Lecture}
- **Processing System**

  Reviews the Cortex™-A72 processor APU and Cortex-R5 processor RPU that form the Scalar Engine. The platform management controller (PMC), processing system manager (PSM), I/O peripherals, and PS-PL interfaces are also covered. {Lecture}
- **PMC and Boot and Configuration**

  Describes the platform management controller, platform loader and manager (PLM) software and boot and configuration. {Lecture, Lab}
- **SelectIO Resources**

  Describes the I/O bank, SelectIO™ interface, and I/O delay features. {Lecture}
- **Clocking Architecture**

  Discusses the clocking architecture, clock buffers, clock routing, clock management functions, and clock de-skew. {Lecture, Lab}
- **System Interrupts**

  Discusses the different system interrupts and interrupt controllers. {Lecture}

Day 2

- **Timers, Counters, and RTC**

  Provides an overview of timers and counters, including the system counter, triple timer counter (TTC), watchdog timer, and real-time clock (RTC). {Lecture}
- **Software Build Flow**

  Provides an overview of the different build flows, such as the do it yourself, Yocto Project, and PetaLinux tool flows. {Lecture, Lab}
- **Software Stack**

  Reviews the Versal ACAP bare-metal, FreeRTOS, and Linux software stack and their components. {Lecture}
- **DSP Engine**

  Describes the DSP58 slice and compares the DSP58 slice with the DSP48 slice. DSP58 modes are also covered in detail. {Lecture}
- **AI Engine**

  Discusses the AI Engine array architecture, terminology, and AIE interfaces. {Lecture}

- **NoC Introduction and Concepts**
  Covers the reasons to use the network on chip, its basic elements, and common terminology. {Lecture, Lab}
- **Device Memory**
  Describes the available memory resources, such as block RAM, UltraRAM, LUTRAM, embedded memory, OCM, and DDR. The integrated memory controllers are also covered. {Lecture}
- **Programming Interfaces**
  Reviews the various programming interfaces in the Versal ACAP. {Lecture}
- **Application Partitioning**
  Covers what application partitioning is and how the mapping of resources based on the models of computation can be performed. {Lecture}

Day 3

- **PCI Express & CCIX**
  Provides an overview of the CCIX PCIe module and describes the PL and CPM PCIe blocks. {Lecture, Lab}
- **Serial Transceivers**
  Describes the transceivers in the Versal ACAP. {Lecture}
- **Power and Thermal Solutions**
  Discusses the power domains in the Versal ACAP as well as power optimization and analysis techniques. Thermal design challenges are also covered. {Lecture}
- **Debugging**
  Covers the Versal ACAP debug interfaces, such as the test access port (TAP), debug access port (DAP) controller, and high-speed debug port (HSDP). {Lecture, Lab}
- **Security Features**
  Describes the security features of the Versal ACAP. {Lecture}
- **System Simulation**
  Explains how to perform system-level simulation in a Versal ACAP design. {Lecture, Lab}
- **System Design Methodology**
  Reviews the Xilinx-recommended methodology for designing a system. {Lecture}

Register Today

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