Designing with the Versal ACAP: Network on Chip

ACAP 2

ACAP-NOC (v1.0H)

Course Specification

Course Description

This course introduces the Versal™ ACAP network on chip (NoC) to users familiar with Xilinx devices. Besides providing an overview of the major components in the Versal device, the course illustrates how the NoC is used to efficiently move data within the device.

The emphasis of this course is on:

- Enumerating the major components comprising the NoC architecture in the Versal ACAP
- Implementing a basic design using the NoC
- Configuring the NoC for efficient data movement

Level – ACAP 2

Course Duration – 1 day

Price – $900 or 9 Training Credits

Course Part Number – ACAP-NOC

Who Should Attend? – Hardware developers and system architects whether migrating from existing Xilinx devices or starting out with the Versal ACAP devices

Prerequisites

- Any Xilinx device architecture class
- Familiarity with the Vivado® Design Suite

Software Tools

- Vivado Design Suite 2020.2

Hardware

- Architecture: Xilinx Versal ACAPs

After completing this comprehensive training, you will have the necessary skills to:

- Identify the major network on chip components in the Versal ACAP
- Include the necessary components to access the NoC from the PL
- Configure connection QoS for efficient data movement

Course Outline

- **Architecture Overview for Existing Xilinx Users**
  Introduces to students that already have familiarity with Xilinx architectures to the new and updated features found in the Versal ACAP devices. {Lecture}
- **Versal ACAPs Compared to Zynq UltraScale+ Devices**
  The Versal ACAP has a number of similarities to the Zynq® UltraScale+™ MPSoC devices. Understanding what is the same, what is different, and what is brand new helps put this powerful new part into context. {Lecture}
- **NoC Introduction and Concepts**
  Reviews the basic vocabulary and high-level operations of the NoC. {Lecture, Lab}
- **NoC Architecture**
  Provides the first deep dive into the sub-blocks of the NoC and how they are used. Describes how the NoC is accessed from the programmable logic. {Lecture}
- **Design Tool Flow Overview**
  Designers come to the Versal ACAP devices with different goals. This module explores how traditional FPGA designers, embedded developers, and accelerated system designers would use the various tools available in the Xilinx toolbox. {Lecture}
- **NoC DDR Memory Controller**
  The integration between the NoC pathways and the DDR memory controllers must be understood to have efficient data movement on and off chip. This discussion of the NoC's DDR memory controller blocks provides the background for properly selecting and configuring DDR memory and the memory controller for effective use. {Lecture}
- **NoC Performance Tuning**
  Synthesizes everything about the NoC and its DDRMCs, illustrating how to fine tune the NoC for the best performance. {Lecture, Lab}
- **System Design Migration**
  Describes how different users will leverage tools and processes to migrate their designs to the Versal ACAP devices. {Lecture}

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