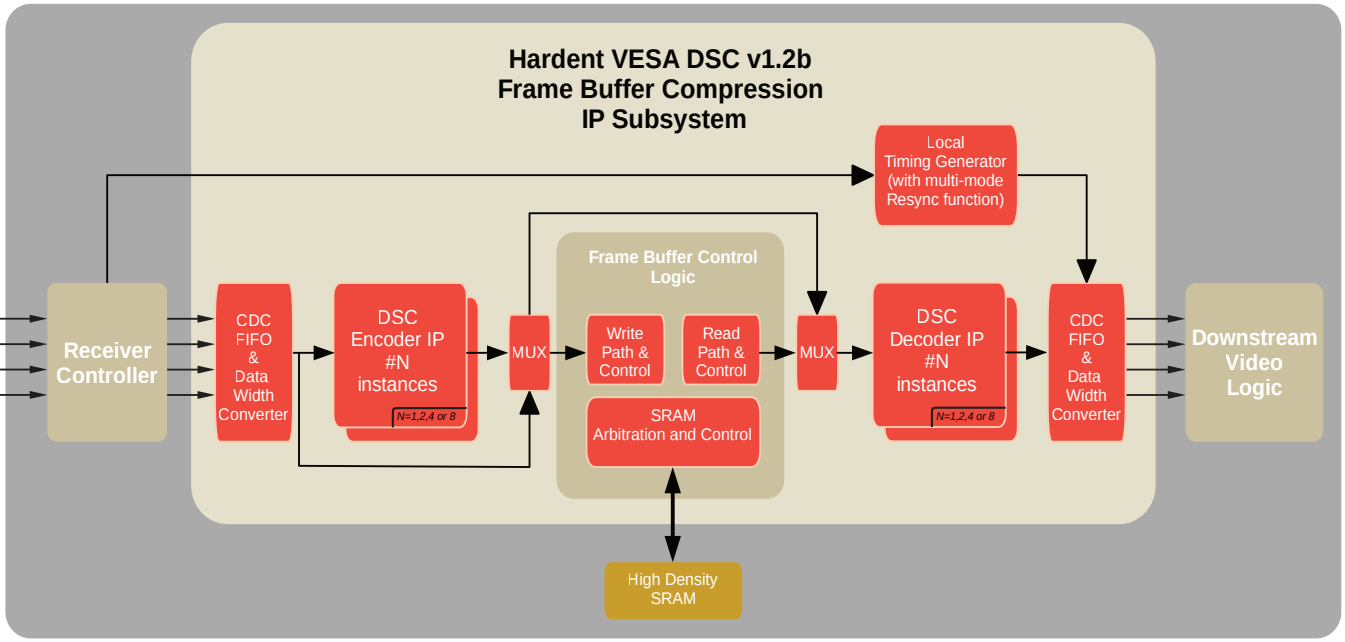
VESA DSC 1.2b Frame Buffer Compression IP Subsystem

Applications

- TCON and PCON ICs with eDP 1.4b /eDP 1.5 / DP™ 2.0 interfaces and supporting Panel Self Refresh (PSR1/PSR2) or Panel Replay
- Laptops and tablets
- Automotive displays



Key Features

- Frame Buffer Compression using VESA® Display Stream Compression (DSC)
  - o Frame buffer area reduction by 66% and more
  - o Visually lossless quality for all types of content
- Includes both DSC v1.2b Encoder and Decoder IPs
  - o Fully compliant DSC IPs (incl. all optional features)
  - o Multiple instances in parallel for increased throughput
  - o Supports display resolutions of 8K (FUHD) at 60 frames per second (fps) and above
- Static RAM control logic with R/W arbitration
  - o Support for single ported RAM
- Partial frame buffer updates (Selective Region Updates) supported
- Single frame buffering with very low latency

Deliverables

- Frame Buffer Compression Subsystem reference design with DSC Encoder & DSC Decoder IPs
- Scripts and timing constraints for FPGA prototyping (Xilinx® or Intel® FPGAs)
- Testbench with integrated checkers to demonstrate functionality (incl. partial frame buffer updates)
- Latest VESA DSC v1.2b C-model and new test case creation scripts
- Detailed documentation for the design and testbench
- Optional ASIC development deliverables:
  - o Synthesis guidelines and timing constraints for front end synthesis
  - o Test plan and structural coverage reports

DSC-FBC-SUB_prodbrief-v1.0

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For additional information contact:
info@hardent.com
+1-514-284-5252
www.hardent.com